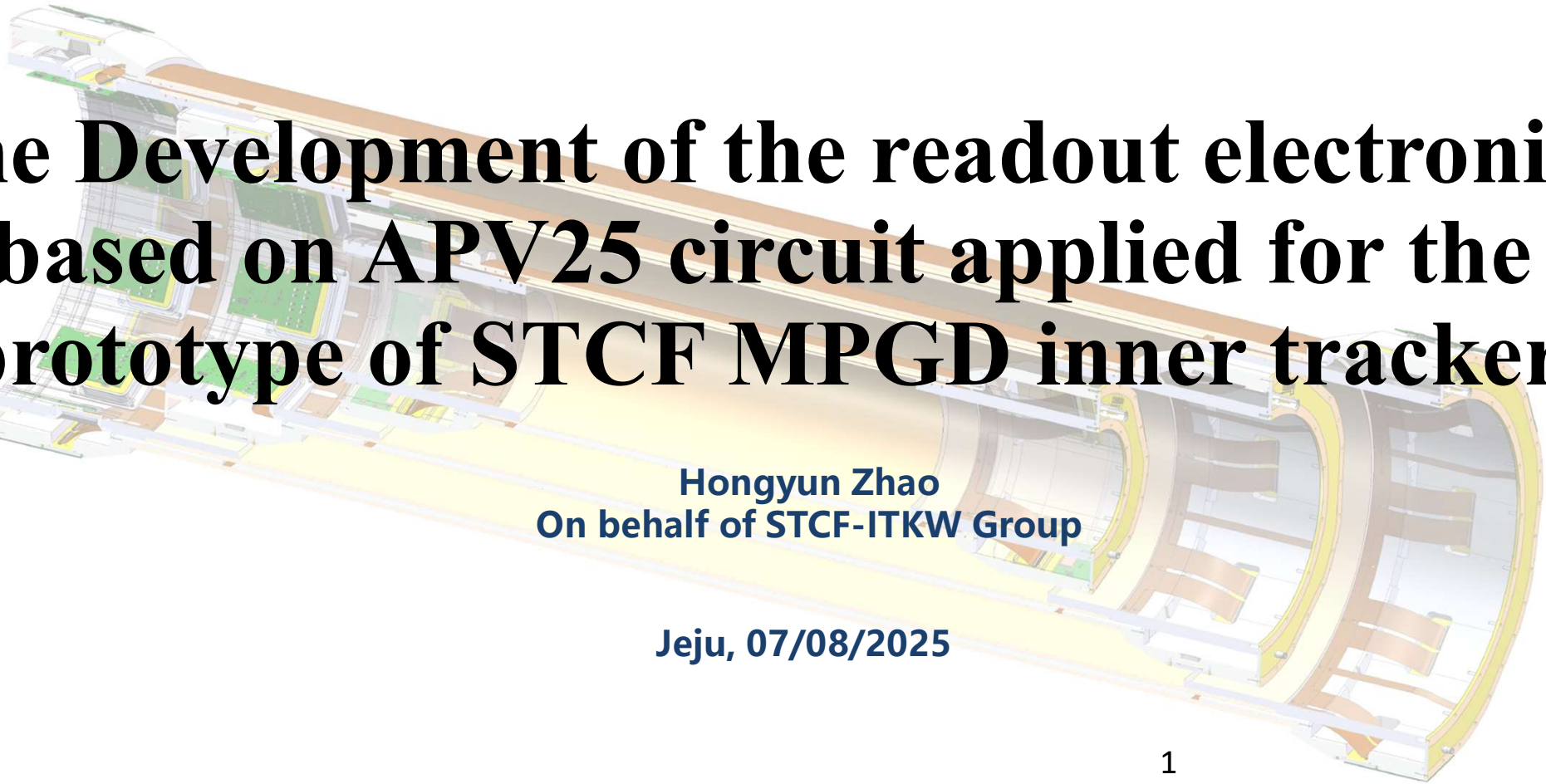


The Development of the readout electronics based on APV25 circuit applied for the prototype of STCF MPGD inner tracker

Hongyun Zhao
On behalf of STCF-ITKW Group

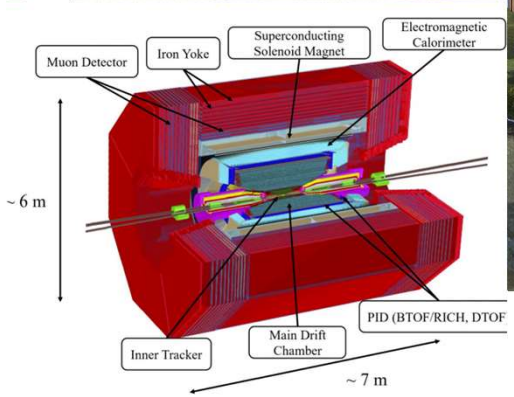
Jeju, 07/08/2025

Outline

- Introduction
- Detector design
- APV25-based Readout electronics
- Front-end ASIC Prototype
- Summary

Super Tau-Charm Facility

STCF is an e + e- collider operating at $\sqrt{s}$=2～7 GeV with a peak luminosity of 0.5×10^{35} cm^{-2}s^{-1}.



ITK
- <0.3%X_0 /layer
- $\sigma_{xy} < 100\mu m$
- Handle high event rate

Cylindrical MPGD
CMOS MAPS

MDC
- $\sigma_{xy} < 130\mu m$
- σ_p/p ~0.5% @ 1GeV
- dE/dX ~6%
- <5%X_0

Cylindrical Drift chamber

PID
- π/K (and K/p) eff>97% Separation up to 2GeV/c

RICH with MPGD
DIRC-like TOF

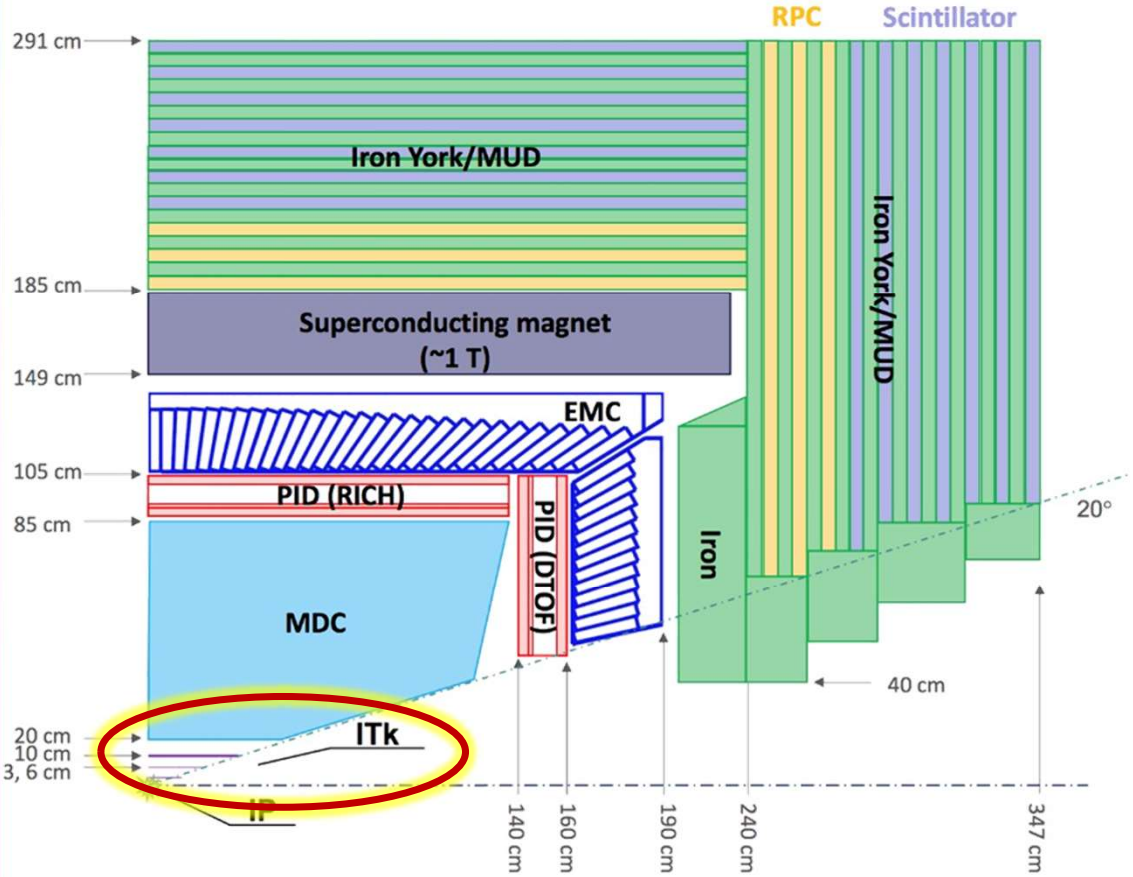
EMC
- E range: 0.025-3.5GeV
- $\sigma_E(\%)@\ 1GeV$
- Barrel: 2.5
- Endcap: 4
- Pos. Res. : 5mm

pCsI + APD

MUD
- 0.4 – 2 GeV
- μ/π suppression >30
- M detection eff>95%@p>0.7GeV/c

RPC + scintillator

The profile of the spectrometer system



Physics Process	Optimized Sub-detector	Requirements
$\tau \to K_s\pi\nu_\tau$, $J/\psi \to \Lambda\bar{\Lambda}$, $D_{(s)}$ tag	Tracker	acceptance: 93% of 4π; trk. effi.: > 99% at $p_T > 0.3$ GeV/c; > 90% at $p_T = 0.1$ GeV/c $\sigma_p/p = 0.5\%$, $\sigma_{\gamma\phi} = 130\ \mu$m at 1 GeV/c
$e^+e^- \to KK + X$, $D_{(s)}$ decays	PID	K/π seperation ($p < 2$ GeV/c): 3σ, efficiency > 99%
$\tau \to \mu\mu\mu$, $D_s \to \mu\nu$	MUC, PID	π/μ suppression power over 30 at $p < 2$ GeV, μ efficiency over 95% at $p = 1$ GeV
$\tau \to \gamma\mu$, $\psi(3686) \to \gamma\eta(2S)$	EMC	$\sigma_E/E \approx 2.5\%$ at 1 GeV $\sigma_{\text{pos}} = 4$ mm at 1 GeV
$e^+e^- \to n\bar{n}$, $D_0 \to K_L\pi^+\pi^-$	EMC, MUC	$\sigma_T = \frac{300}{\sqrt{p^3(\text{GeV}^3)}}$ ps

- **Inner Tracker**
  - MPGD: cylindrical MPGD
  - Silicon: CMOS MAPS

Sensitivity angle: 94%•4π (θ ~ 20°)

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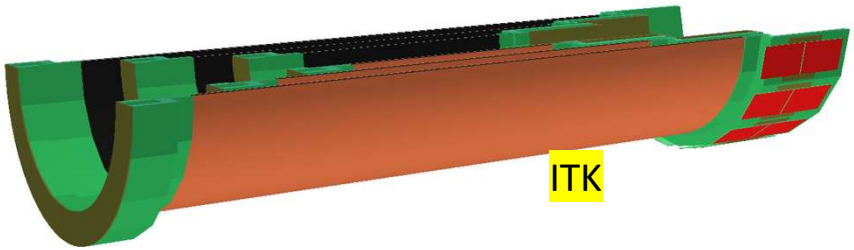
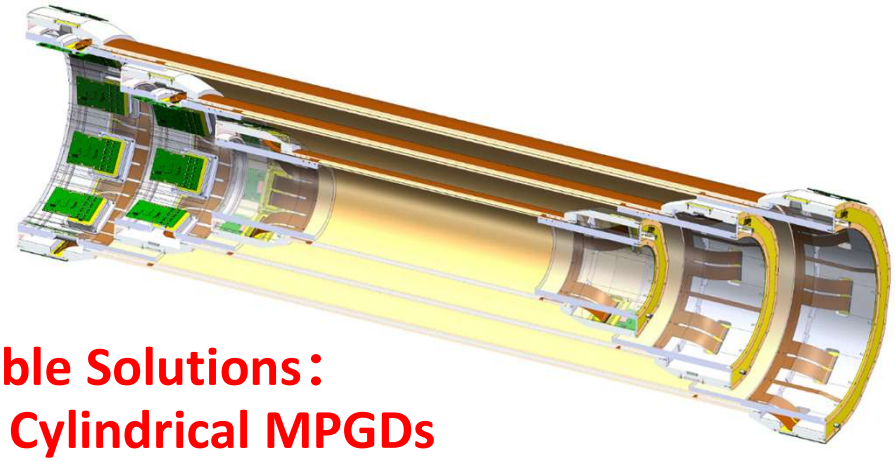
Inner Tracker (ITK)

Track detection under extremely high luminosity requires the **ITK** performance includes:

- **Good Spatial resolution @1T magnetic field (<100μm)**
- **Ultra-Low Material Budget (<0.3%X0)**
- **Handle high counting rate**

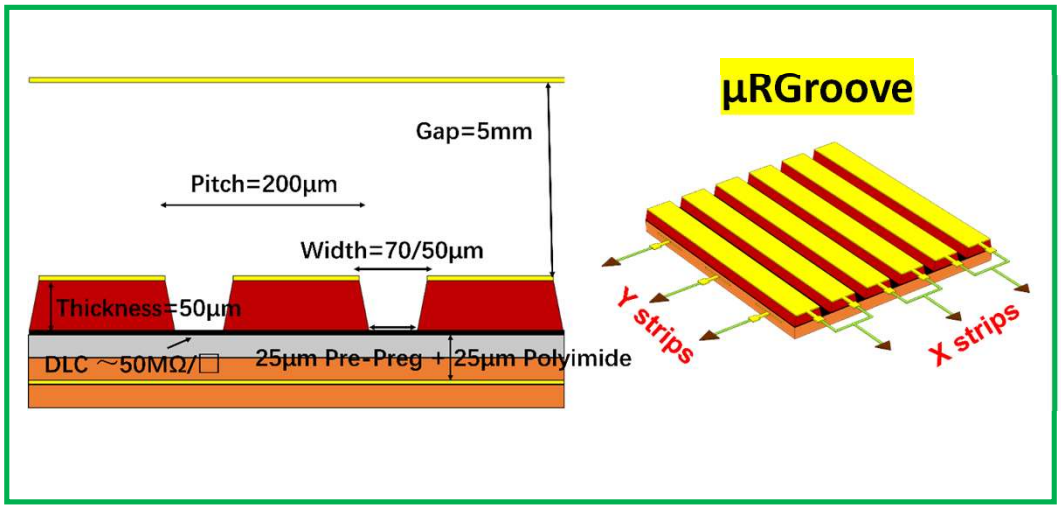


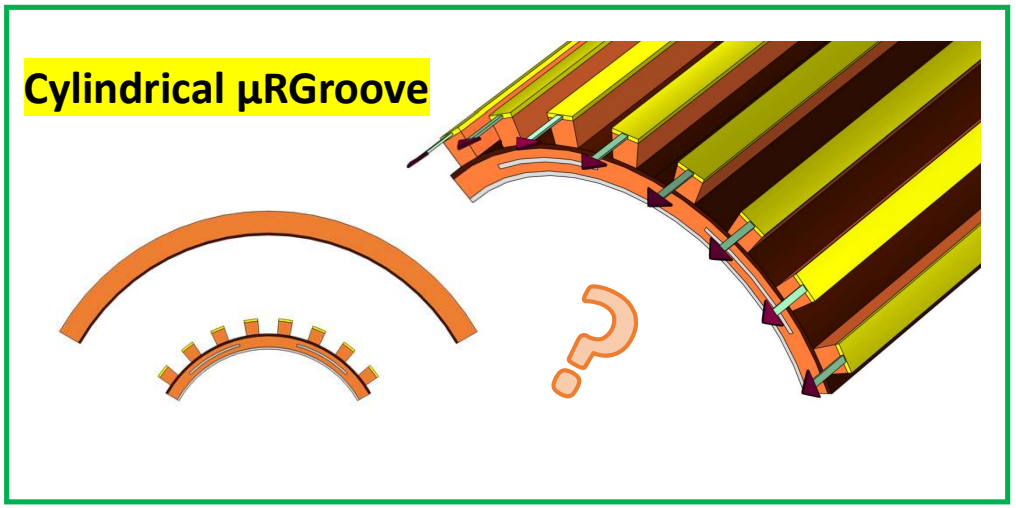
ITK



Possible Solutions:
Cylindrical MPGDs

Micro Resistive Groove (μRGroove) Prototype

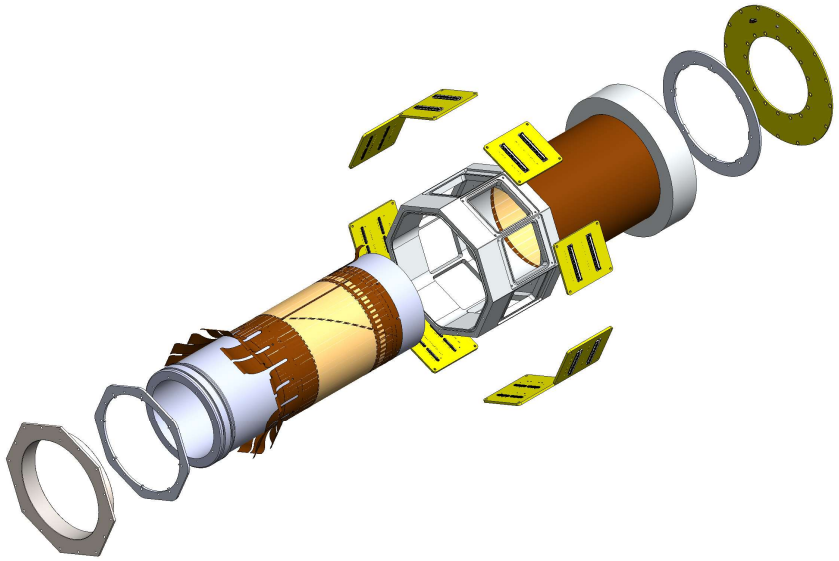


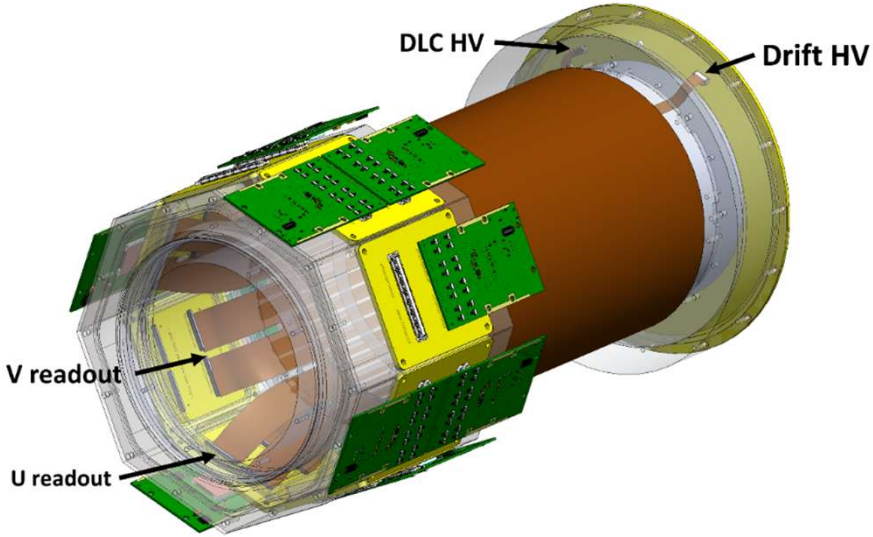


- **The cathode of μRGroove itself can be used as 1D-readout strip.**
  - ✓ Decoupled X&Y readout strips, no induced charge sharing effect, increased signal amplitude.
  - ✓ Easy to produce with low cost;

- **Cylindrical μRGroove:**
  - ✓ **Simple structure:** Only contains drift and μRGroove layer
  - ✓ **Each electrode contains support structure**
  - ✓ **Lower material budget**: Only 1D additional readout strips is needed
  - ✓ **Easy to clean** for long-term maintenance.

Mechanical design





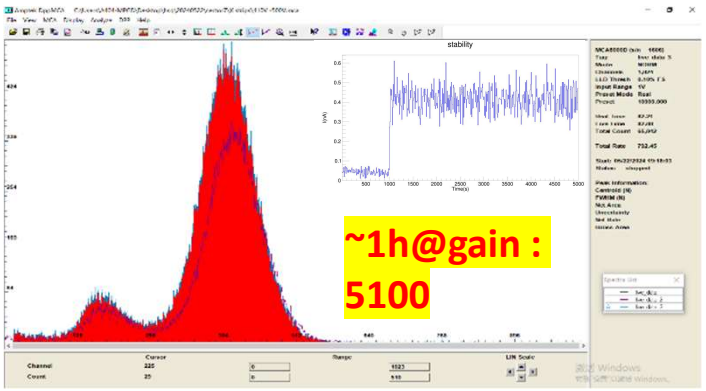
- Aluminum (metal) sleeves benefits grounding and noise shielding.
- Mechanical sealing ensures the detector is detachable
- The spacers provide an uniform 5mm drift gap

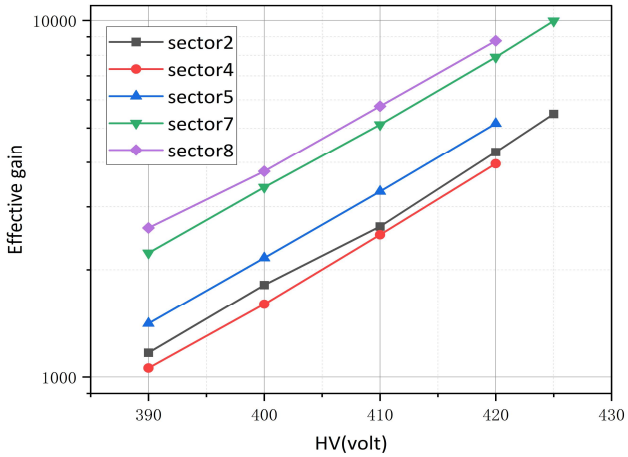
- consists of three parts: FEE side, active area, HV side
- The electrode substrate is flexible and the soft branch can bent up to connect to adapter

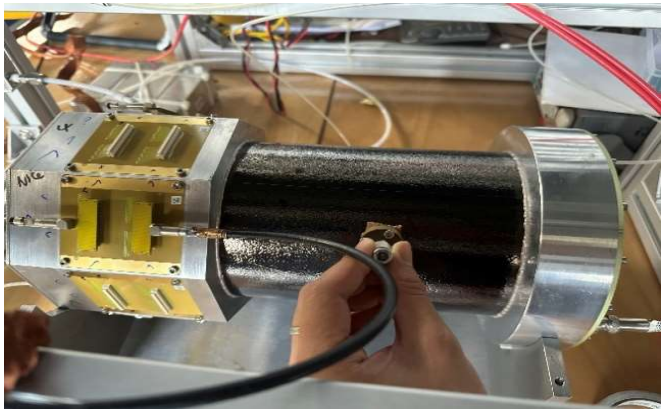
Gain and energy spectrum measurement

Setup：

- Gas: Ar:iC_4H_{10}/95:5
- Source: ^{55}Fe
- Readout from X strips (cathode)
- V strips are grounded
- Ortec142AH/671 + MCA
- Gain measured by signal amplitude spectrum







- ✓ Energy resolution: ~26%;
- ✓ Effective gain: 4000~10000;
- ✓ Similar signal amplitude on X&V readout strips;
- ✓ Good stability if the humidity can keep low enough;
- × Bad gain uniformity, caused by the gas(flow);

Requirements for Electronics

- **Main Requirements for Electronics**
- **Total ch number : 8064, but prototype only needs 1024.**

Read out the electronic index	Requirement
Charge measurement range	20 fC
Time precision	≤10ns @ ≥4.5fC
Integration level / FEE	128Ch
Total number of channels	1024
Event Rate/Ch	> 40 kHz

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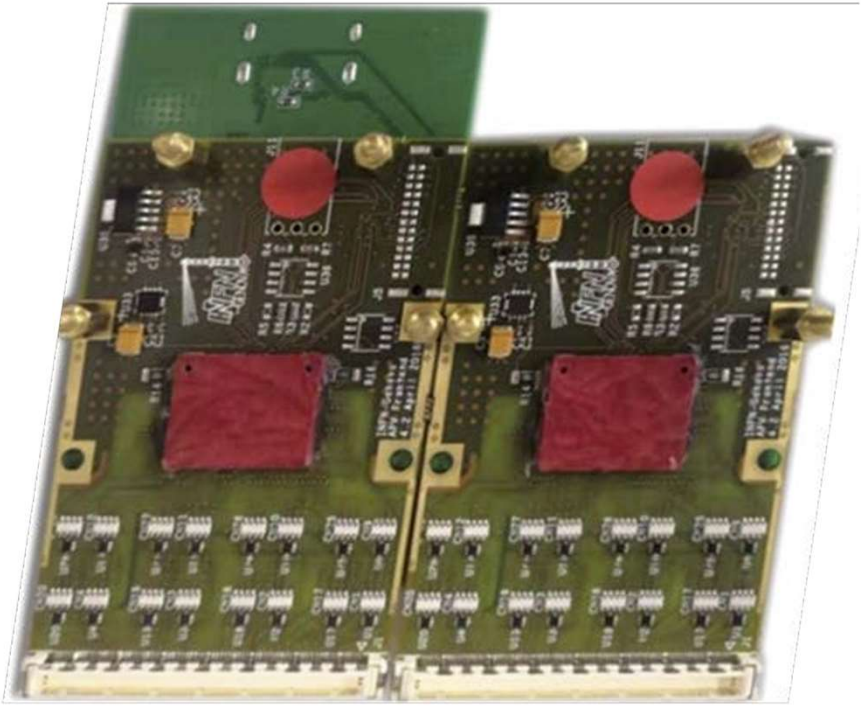
APV25

➢**The advantages of APV25:**

- **The highest Counting rate:280Khz/ch;**
- **Ultra-low power consumption： 2.7mW/ch**
- **Small chip size;**
- **Simple structure and high integration:128ch**
- **Provide the existing ASIC board（INFN）, It can significantly accelerate our research and development progress.**



APV25

Table1. Technical specifications

specifications	value	specifications	value
Process	0.25um CMOS	Analogue pipeline	192 cell
Channel	128	Dynamic range	20fC
Peaking time	50ns	Noise	$270e^{-}+38e^{-}$/pF
Shaper	RC-CR	Power consumption	2.7mW/ch
Preamp polarity	positive, negative	Read-out frequency	20MHz or 40MHz
Sampling rate	40MHz	Output	differential current

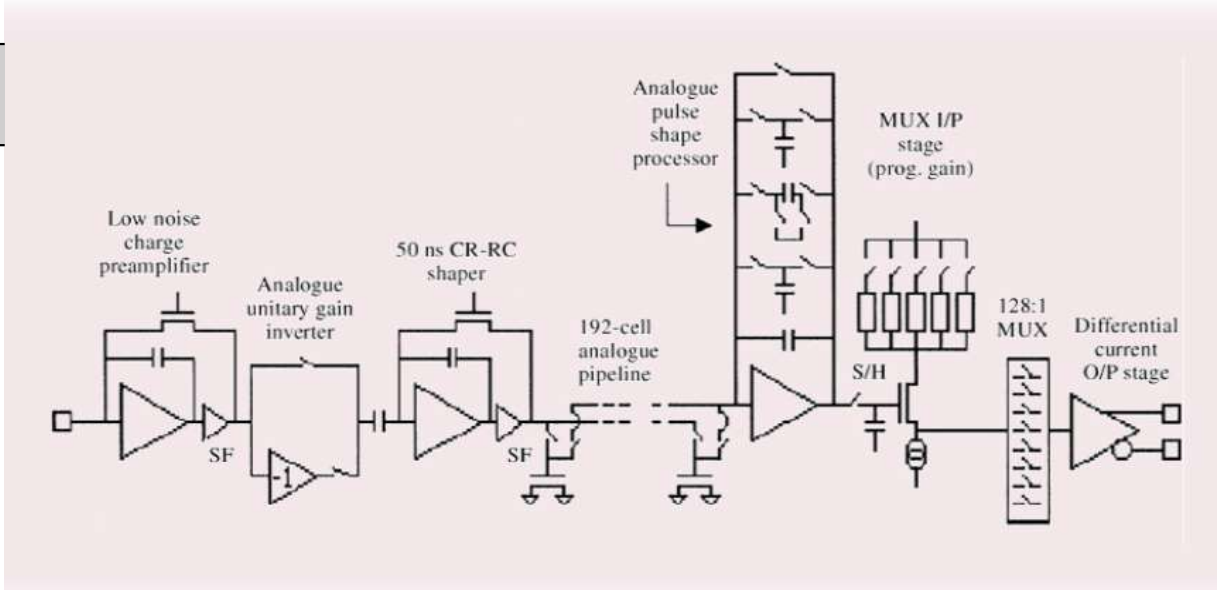


Fig1. Block diagram of one channel of the APV25

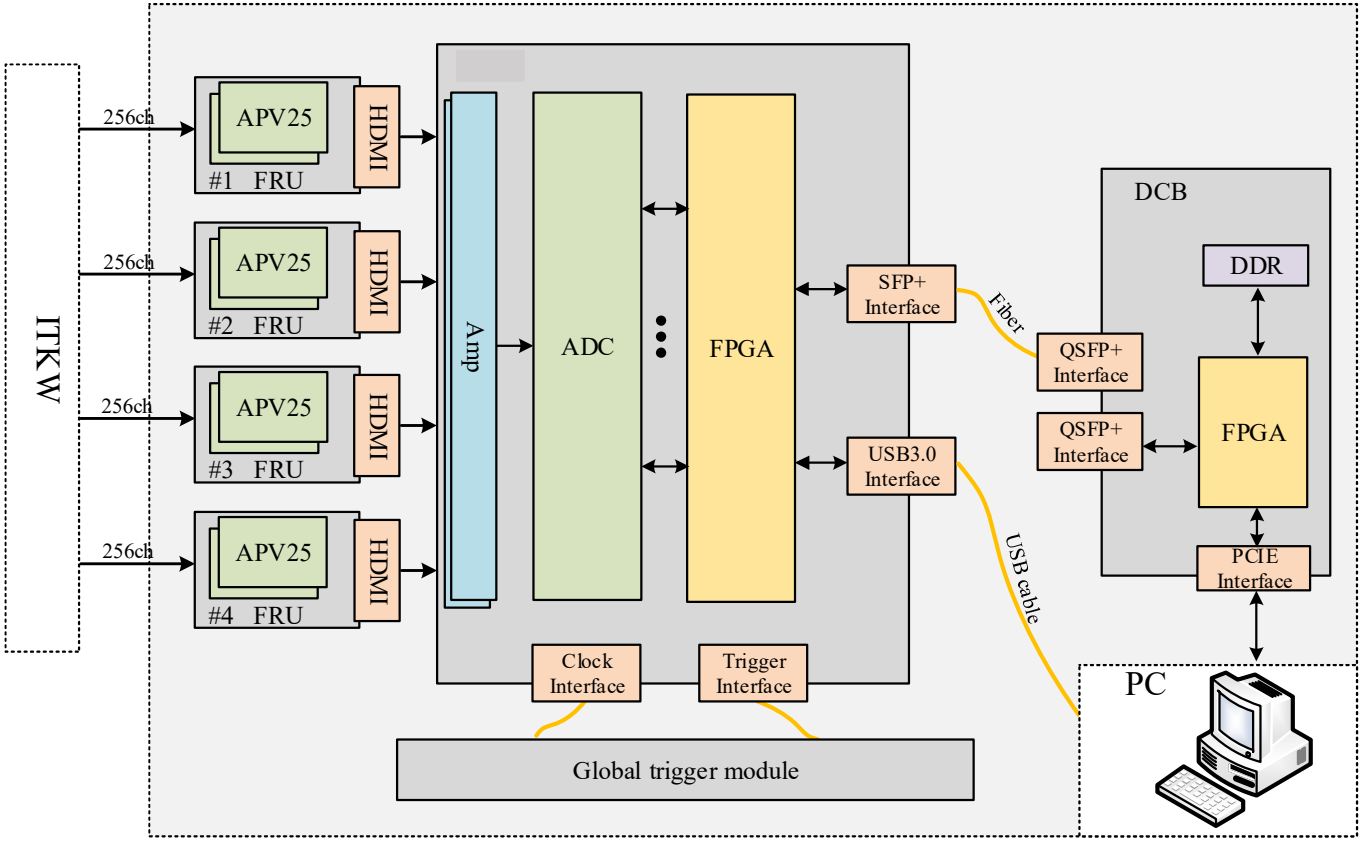
APV25-S1 Mode	Trigger Mode	Read-out Mode
Deconvolution	3-sample	Deconvolution
Peak	1-sample	Peak
Multi	3-sample	Peak

Table2.APV25 read-out mode

1024-channel Readout prototype system

System composition:

- 4 ASIC boards units(2ASIC brd/unit),connected to the FEE board via the HDMI interface;
- 1 FEE board carries ADC and FPGA chips,The FEE board can be connected to the data aggregation board via SFP
- The data aggregation board is connected to the server via the PCIE interface

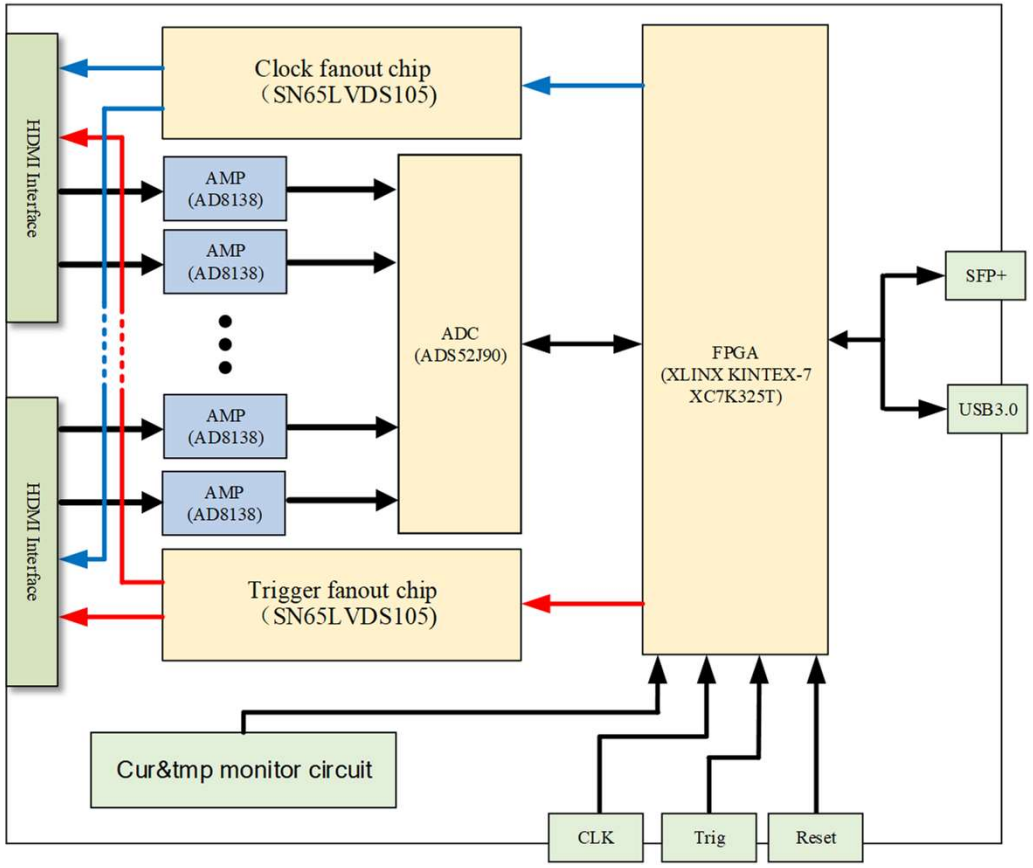


1024ch prototype based on APV25

Hardware design of FEE

◆ FEE Hardware design

- High-performance FPGA and its peripheral circuits(Kintex-7 XC7K325)
- ADC digital circuit(ADS52J90)
- Differential amplifier circuit(AD8138)
- Clock trigger circuit(SI9102, SN65LVDS104)
- Data transmission interface circuit(HDMI, SFP+, USB3.0)



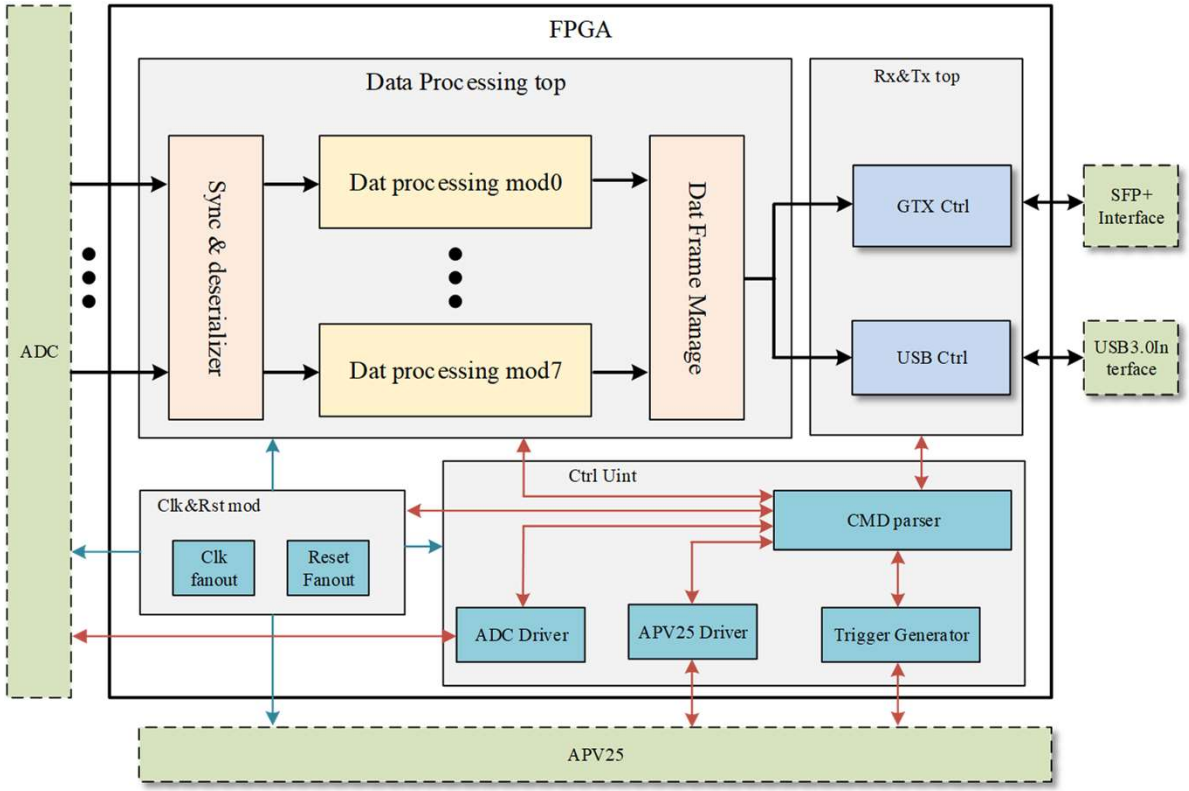
FEB 硬件设计框图

Firmware design for FEE

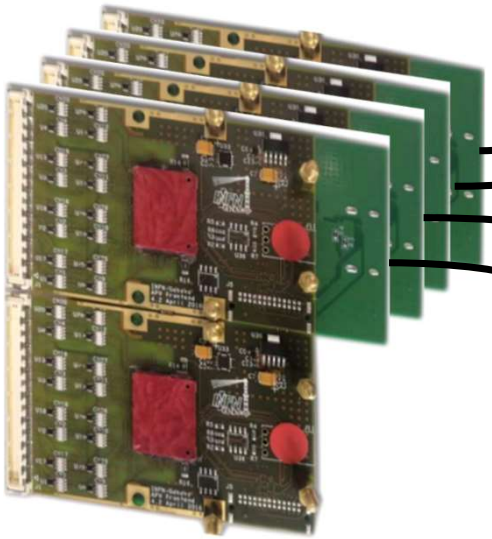
◆FEE Firmware design

The overall framework design of the firmware is shown in the figure below and can be divided into:

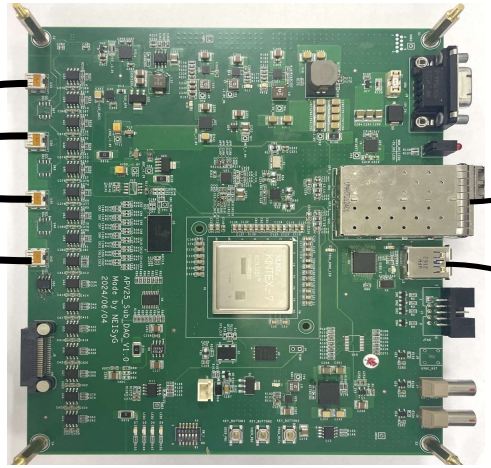
- Control Unit(Instruction Parser, ADC Driver, APV25 Driver, and Trigger Management Module)
- Data Processing Unit(Synchronization and Deserialization, Frame Scheduling and Data Processing Subunits)
- Data Reception and Transmission Unit(GTX Reception and Transmission Controller Module and USB Reception and Transmission Controller Module)
- Clock and Reset Unit(Clock Fanout and Reset Fanout Modules)



APV25-based readout electronics prototyping



ASIC Card



Front-end electronics Card

Slave DAQ

- Modular design： ASIC Card + FEE Card + Slave DAQ
- Scalable
- ASIC Card : 128 channels
- FEB Card : 128x4x2 = 1024 channels
- Slave DAQ: 1024x8 = 8192channels(max support)

Test-8ASIC Card + 1 FEE Card + 1 Slave DAQ

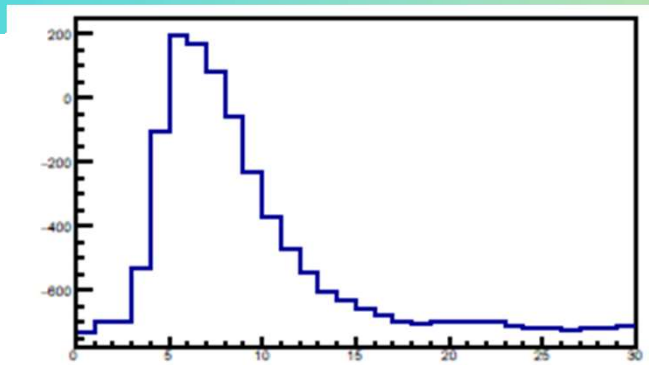
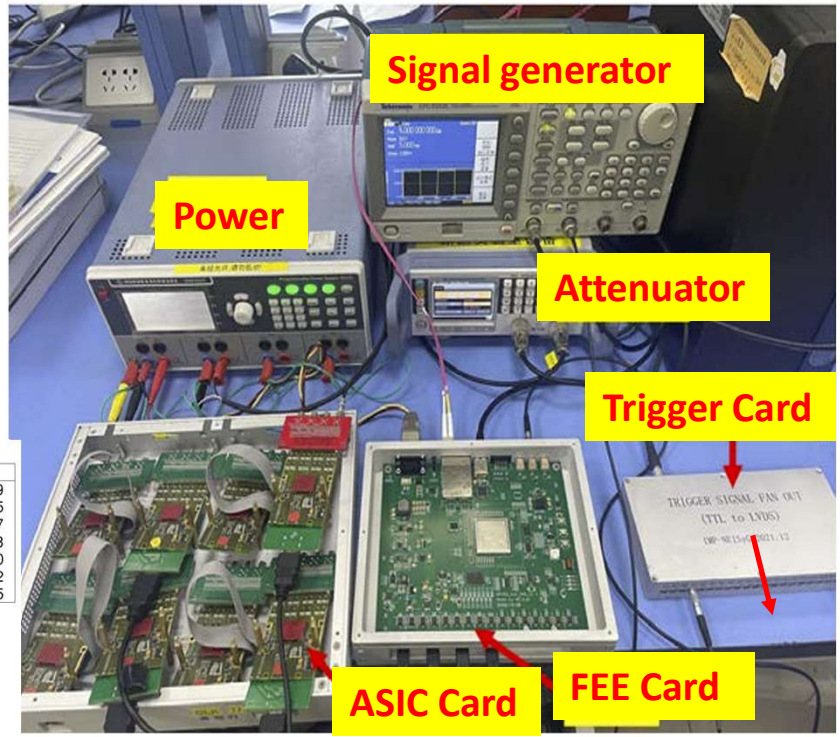


Fig1.Extracted waveforms



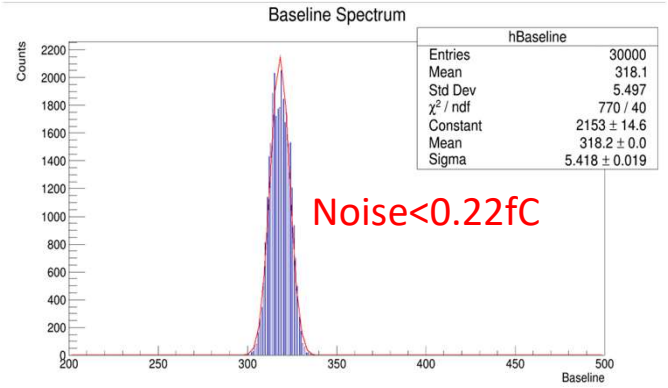


Fig2. Baseline tests

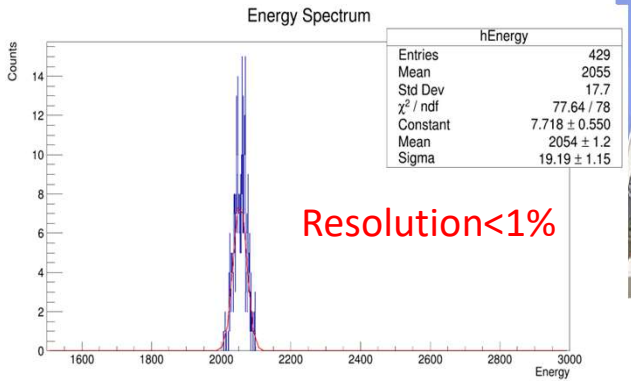
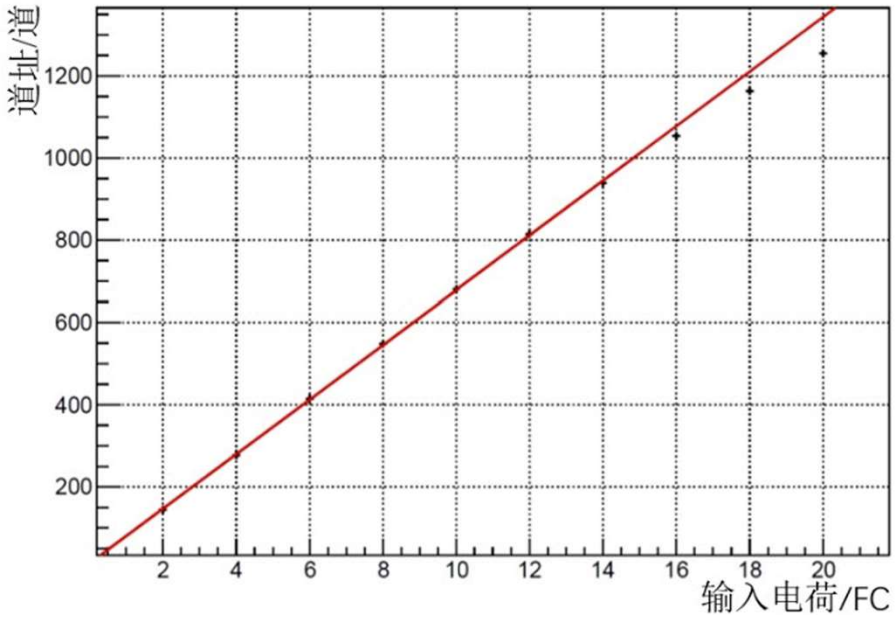
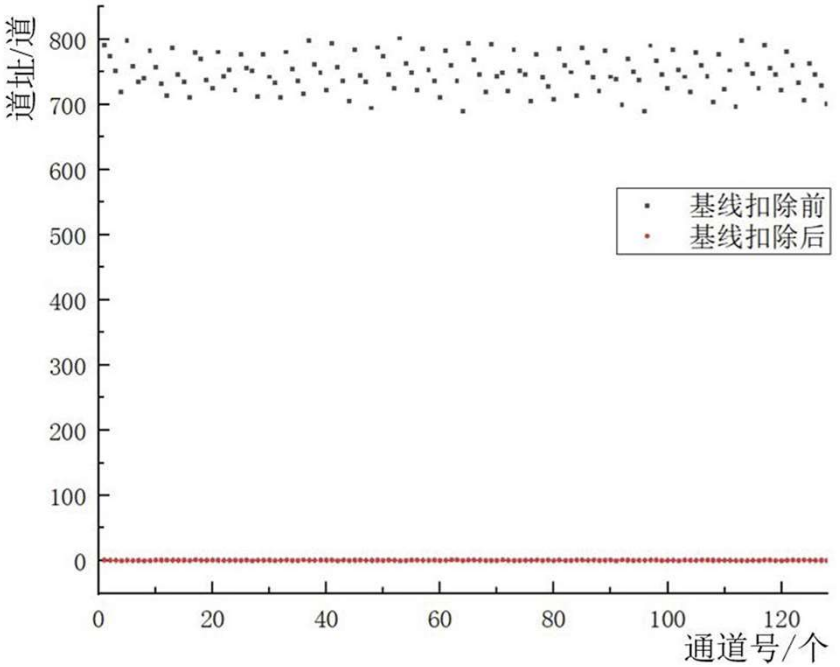


Fig3.Energy Spectrum(20fC)

Test- 4 ASIC Card + 1 FEE Card + 1 Slave DAQ

- From 0 to 12fC, the linear fitting is better than 0.26%. However, in the 12-20fC range, signal amplification has already shown significant distortion, and the performance has deteriorated compared to before. This has been proven in related papers.
- Channel consistency compensation test: Through baseline compensation method, it is possible to effectively eliminate the differences between channels.





Outline

- Introduction
- Detector design
- APV25-based Readout electronics
- **Front-end ASIC Prototype**
- Summary

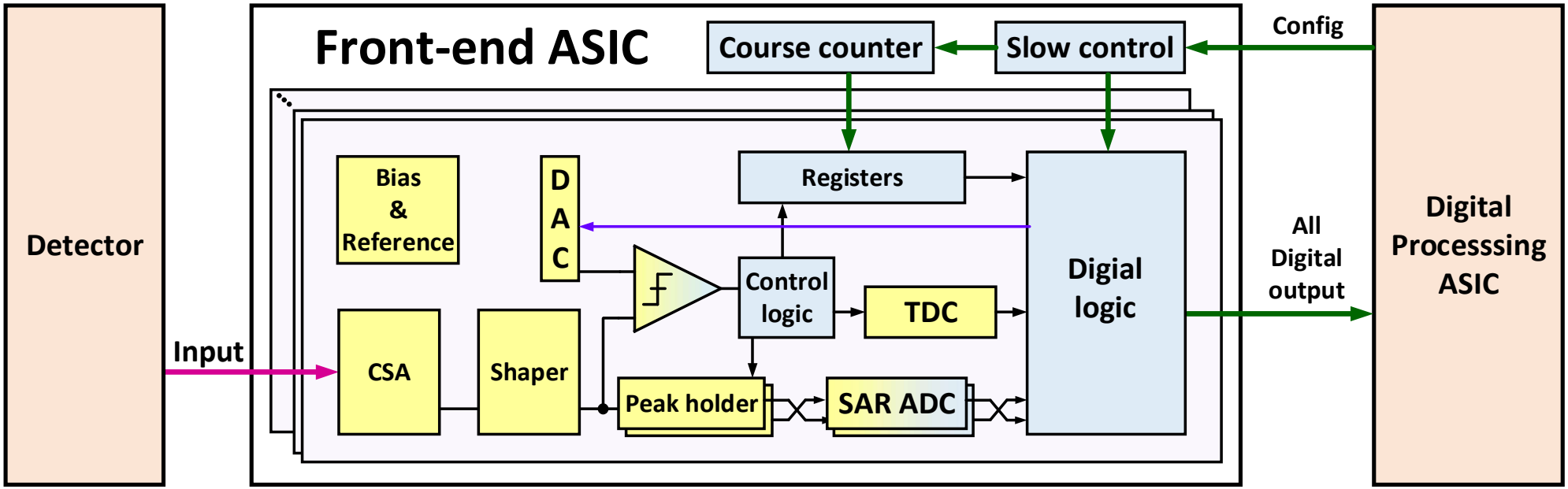
Requirements of Front-end ASIC

- **To meet the high-density and compact readout requirements of MPGD Inner TracKer (ITK), it is necessary to use the Application Specific Integrated Circuit (ASIC).**
  - **High integration → 32 channels (prototype) → 64 channels (final), and digital output.**
  - **Capability of high counting rate → Address high counting rate challenge of ITK under high luminosity.**

Parameters	Requirements
Channels per chip	64 channels (final version)
Maximum counting rate per channel	4 MHz
Charge measurement range	40 fC
Charge resolution	~1 fC (RMS)
Time resolution	<=10 ns (RMS)

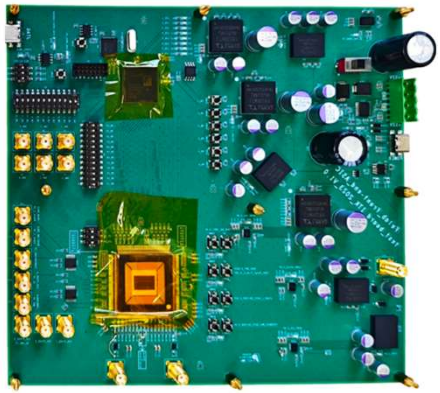
Block diagram of ASIC

- Charge Sensitive Amplifier (CSA) + Shaper for low-noise and high-gain amplification.
- Peak holder + Analog-to-Digital Converter (ADC) for charge measurement.
- Discriminator + Time-to-Digital Converter (TDC) for time measurement.

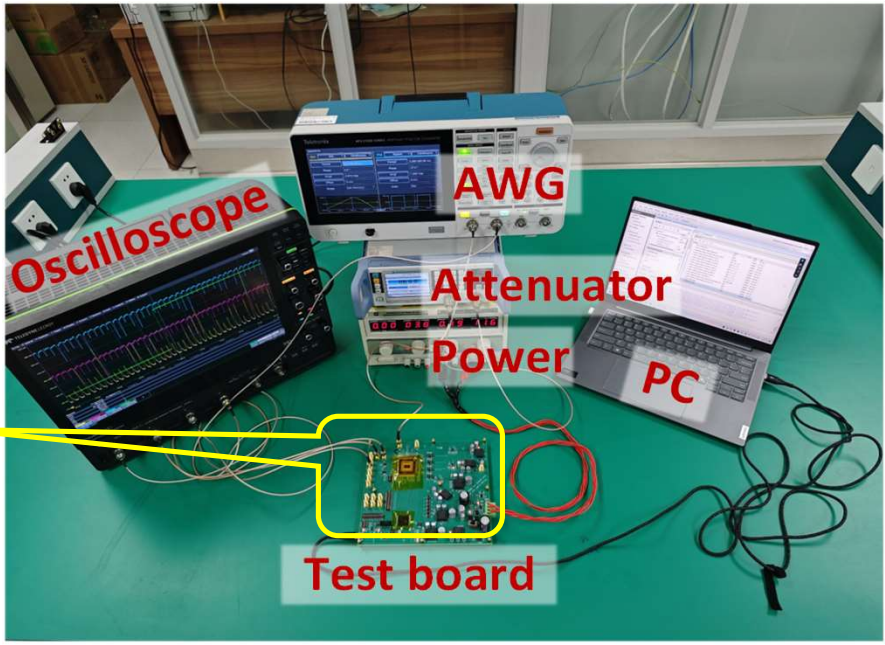


Test Setup

Parameters	value
Channels per chip	32
Peaking time	40ns
Dynamic range	40fC
ADC resolution	6 bits
DAC resolution	8 bits
Threshold range	0~5fC



Test board

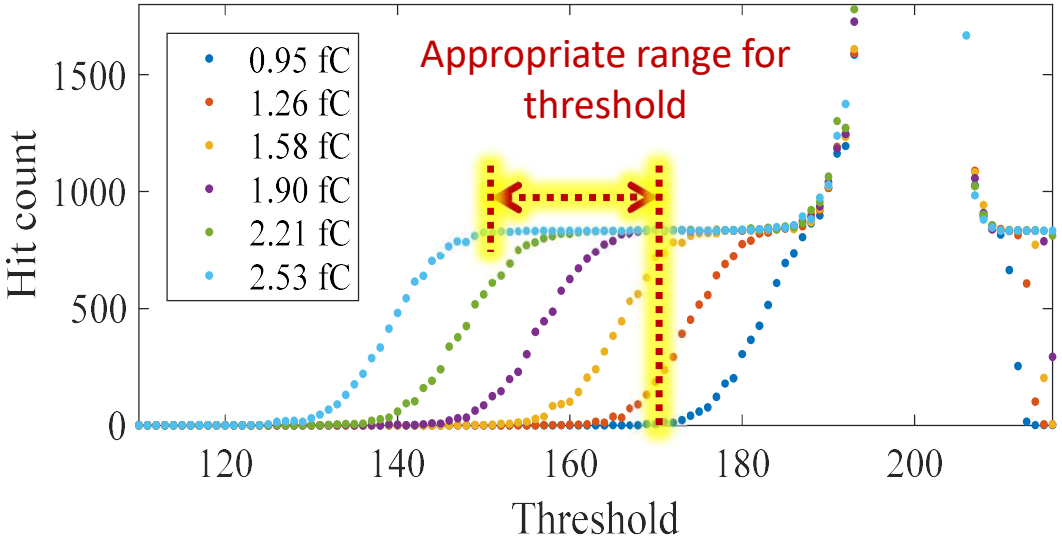


Test site

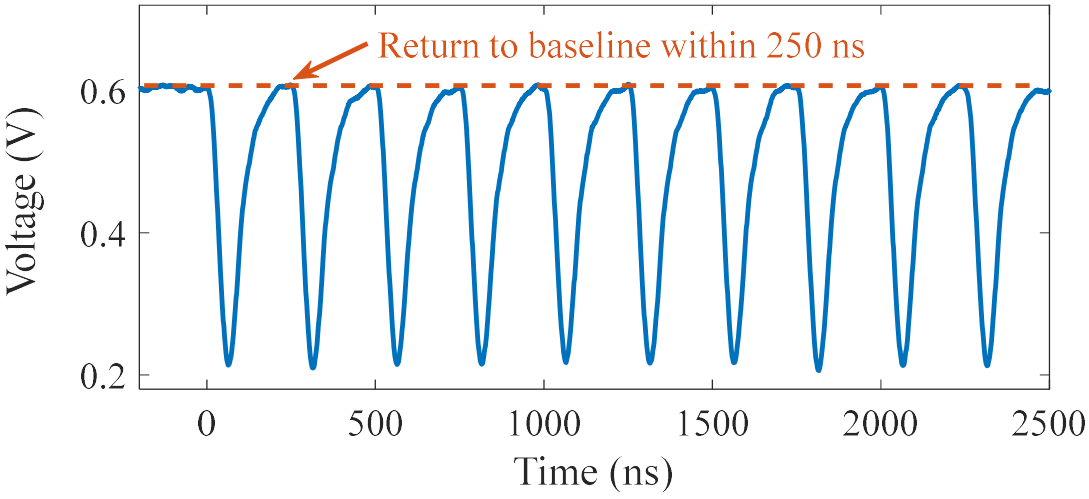
Test Results

- **High detection efficiency and low noise hit rate can be achieved for a 2.5 fC signal when the threshold is set in the range of 150 to 170.**
- **No pile-up between adjacent signals at 4 MHz counting rate.**

Parameters	Requirements
Maximum counting rate per channel	4 MHz
Charge resolution	~1 fC (RMS)
Time resolution	<=10 ns (RMS)



Number of hits under different thresholds for various input charge @ 35 pF C_{in} @ 75 ns charge collection time

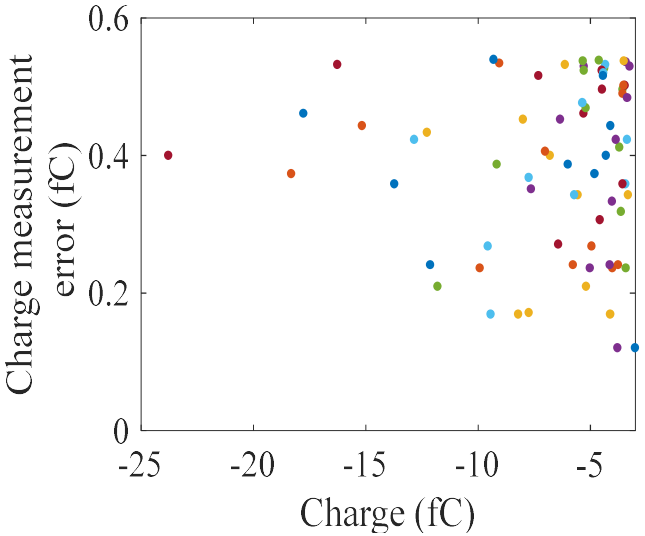


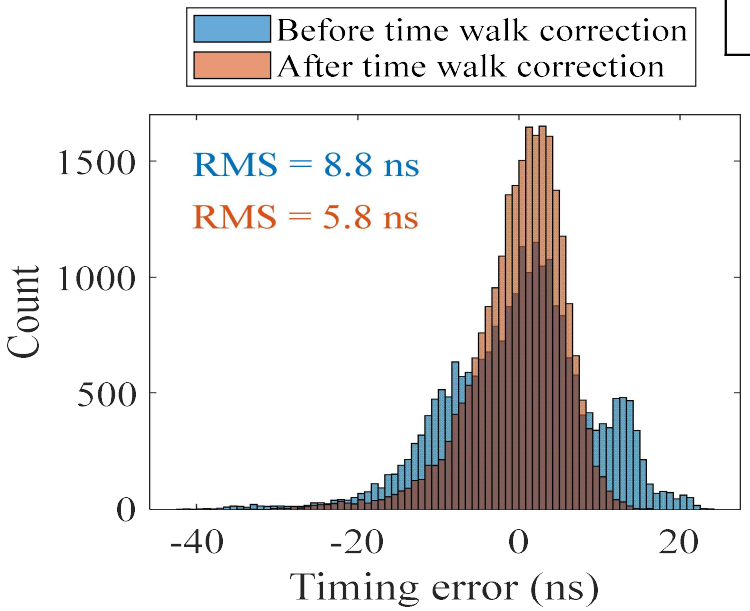
Output waveforms for 4 MHz input signals @ 35 pF C_{in} @ 75 ns charge collection time

Test Results

- **GENT4 simulated waveforms are used as inputs.**
- **Test results show that both charge resolution and time resolution satisfy the design requirements.**

Parameters	Requirements
Maximum counting rate per channel	4 MHz
Charge resolution	~1 fC (RMS)
Time resolution	<=10 ns (RMS)

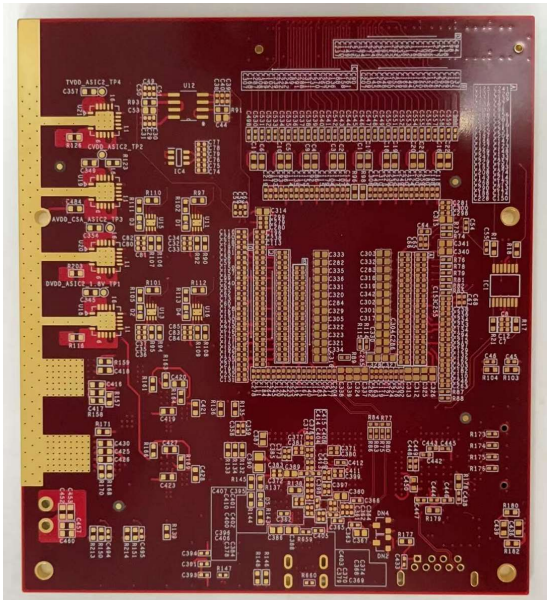


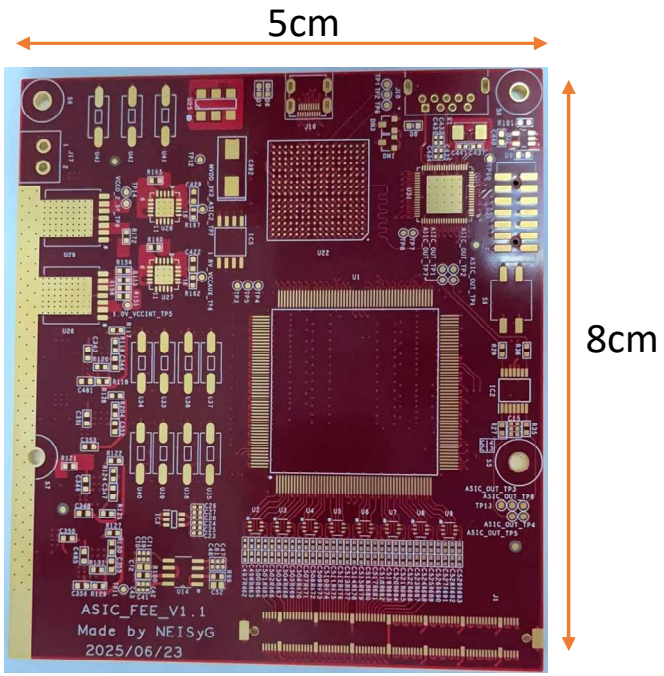


Next work Plan

- Use the APV25 readout electronics to finish the joint test with uGroove detector
- Finish stcf-ASIC board test compare to the APV25 board.

In the first stage, we only designed the intermediate version of the prototype, with only 32 channels. The purpose was to understand the functionality and performance of the ASIC, especially in terms of power consumption.





Final Parameters	Requirements
Total ch	128
high	5cm
width	8cm

Outline

- Introduction
- Detector design & test
- APV25-based Readout electronics design & test
- Front-end ASIC Prototype design & test
- **Summary**

Summary

- Completed the 1st C-µRGroove prototype production and testing with traditional Electronics plugins
- Deisgned the APV25-based readout electronics prototype and finished several tests
- Completed front-end ASIC prototyping and preliminary testing
- Make the improvements mentioned above.