中国科学院近代物理研究所
Institute of Modern Physics, Chinese Academy of Sciences

The 4th Korea-China Workshop for Rare Isotope Physics

The development of front-end readout electronics for CEE-TPC

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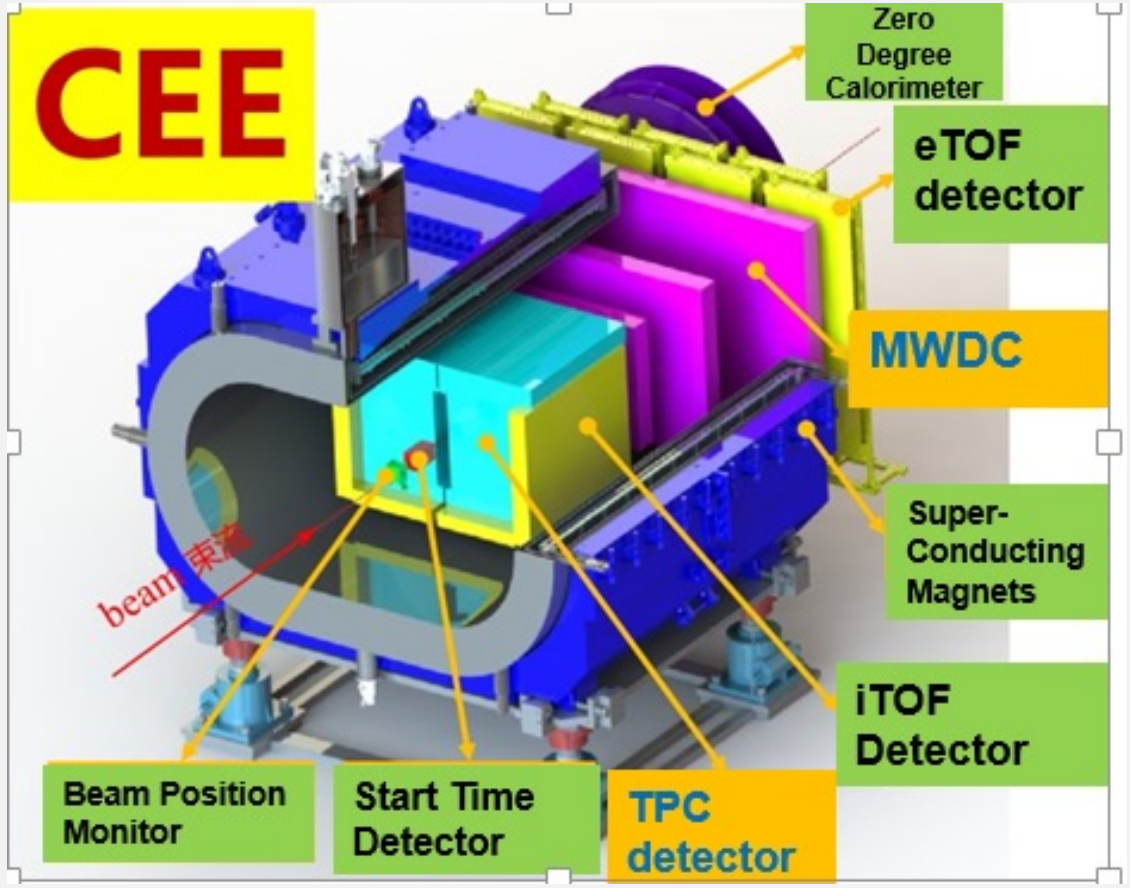
Outline

- Overview
- SAMPA electronics for CEE-TPC
- Summary

Overview

CEE: CSR External-Target Experiment, in Lanzhou China.

It will be the first-large nuclear physics experimental device at HIRFL-CSR



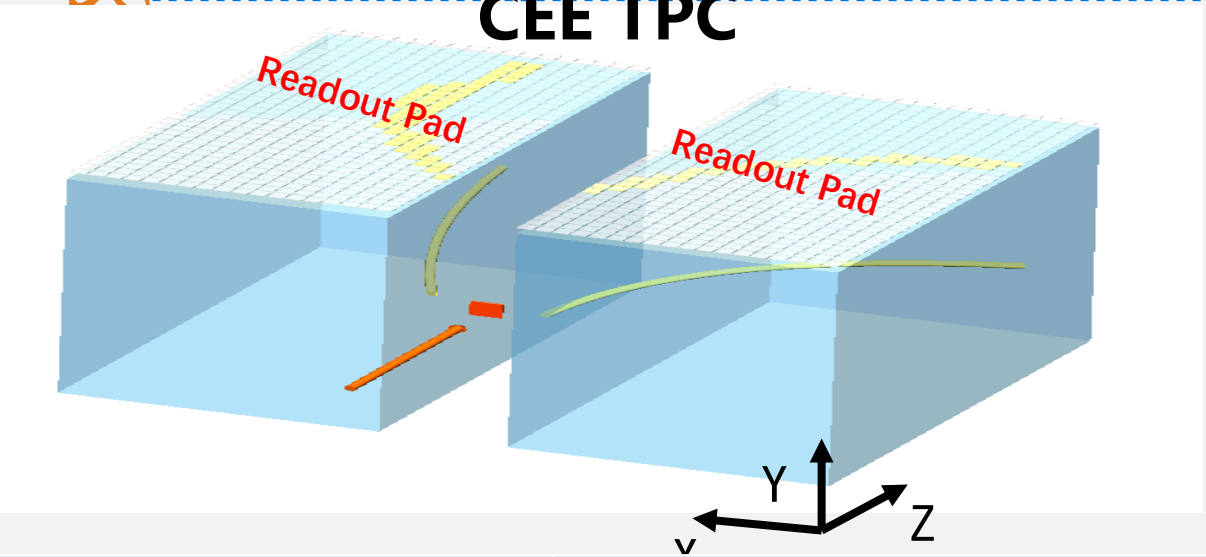
Physical goals

- ➢To study the bulk properties of strongly interacting matter
- ➢To study equation of state high baryon density region
- ➢To understand the quantum chromo dynamics (QCD) phase diagram

A wide acceptance TPC：

- ➢ the core detectors
- ➢ the three-dimensional track measurement with lightly charged particles
- ➢ lightly charged particle identification

CEE TPC



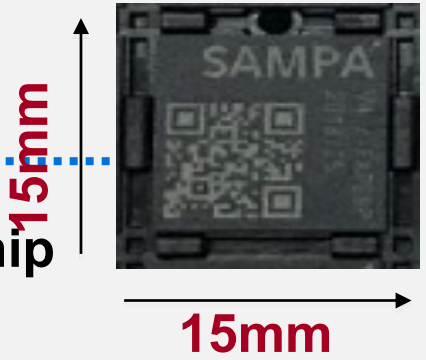
Parameter	Index requirements
Effective sensitive area	500 mm (X) × 800 mm (Y)× 900 mm (Z)
the types of particles	π, p, d, t, ^{3}He, ^{4}He, Li
Resolution of position	$\sigma_{r\phi}$≤500 μm, σ_y≤600 μm
Momentum resolution	The typical relative momentum resolution of π, p is 5%
Nunber of channel	≥10000
Level 1 triggers	1 kHz

Performance Indexes of the Readout Electronics

Parameter	Index requirements
Number of channels	15000
MIP	1.4fc
Signal-to-noise ratio	8：1
Shaping Time	160ns
ENC/ Cd=0pF	<1000e
Dynamic range	1.2fC-110fC
Events Rate	10K event/s

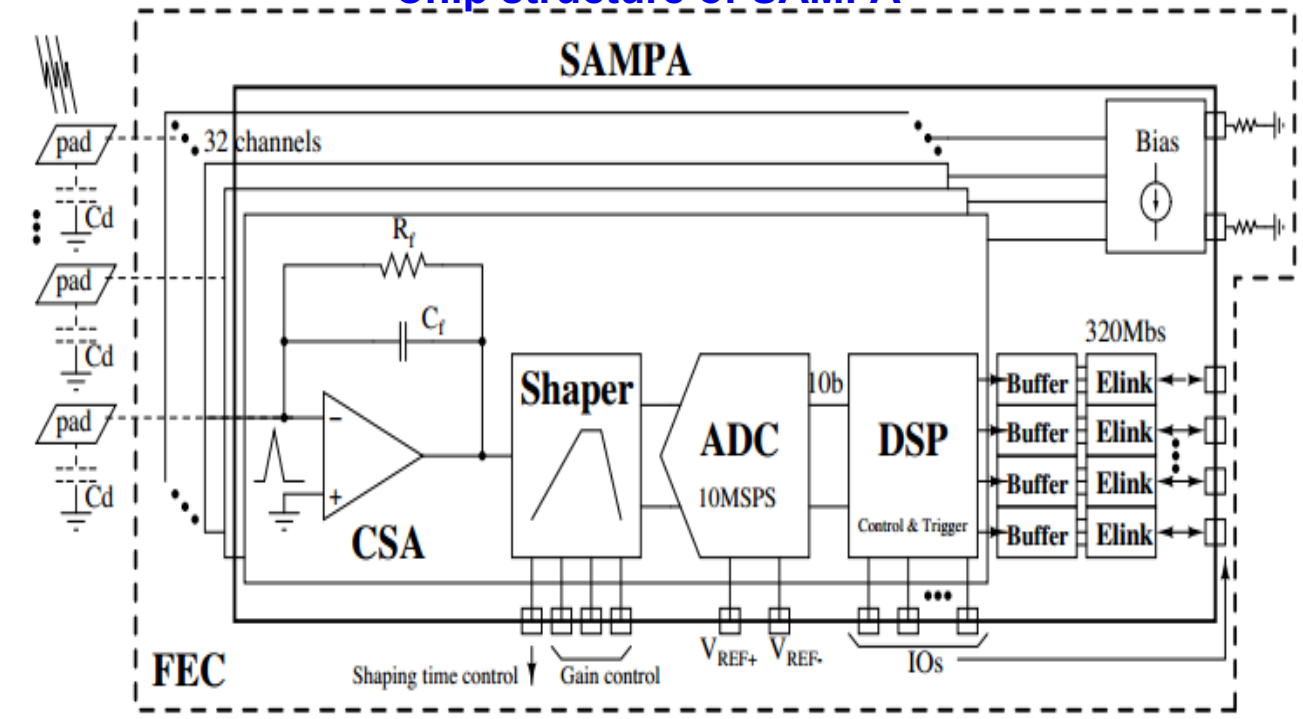
Requirement：high count rate, high integration, low power consumption

SAMPA chip



The SAMPA chip is a large-scale analog and digital mixed-signal ASIC chip developed for Alice TPC front-end readout electronics specifically.

Chip structure of SAMPA



Original specifications of SAMPA

Specification	TPC
Voltage supply	1.25 V
Polarity	Negative
Detector capacitance (Cd)	18.5 pF
Peaking time (ts)	160 ns
Shaping order	4th
Equivalent Noise Charge (ENC)	< 600 e@ts = 160 ns*
Linear Range	100 fC or 67 fC
Sensitivity	20 mV/fC or 30 mV/fC
Non-Linearity (CSA + Shaper)	< 1%
Crosstalk	< 0.3%@ts = 160 ns
ADC effective input range	2 Vpp
ADC resolution	10-bit
Sampling Frequency	10 (20) Msamples/s
INL (ADC)	< 0.65 LSB
DNL (ADC)	< 0.6 LSB
ENOB (ADC)**	> 9.2-bit
Power consumption (per channel) CSA + Shaper + ADC	< 15 mW
Channels per chip	32

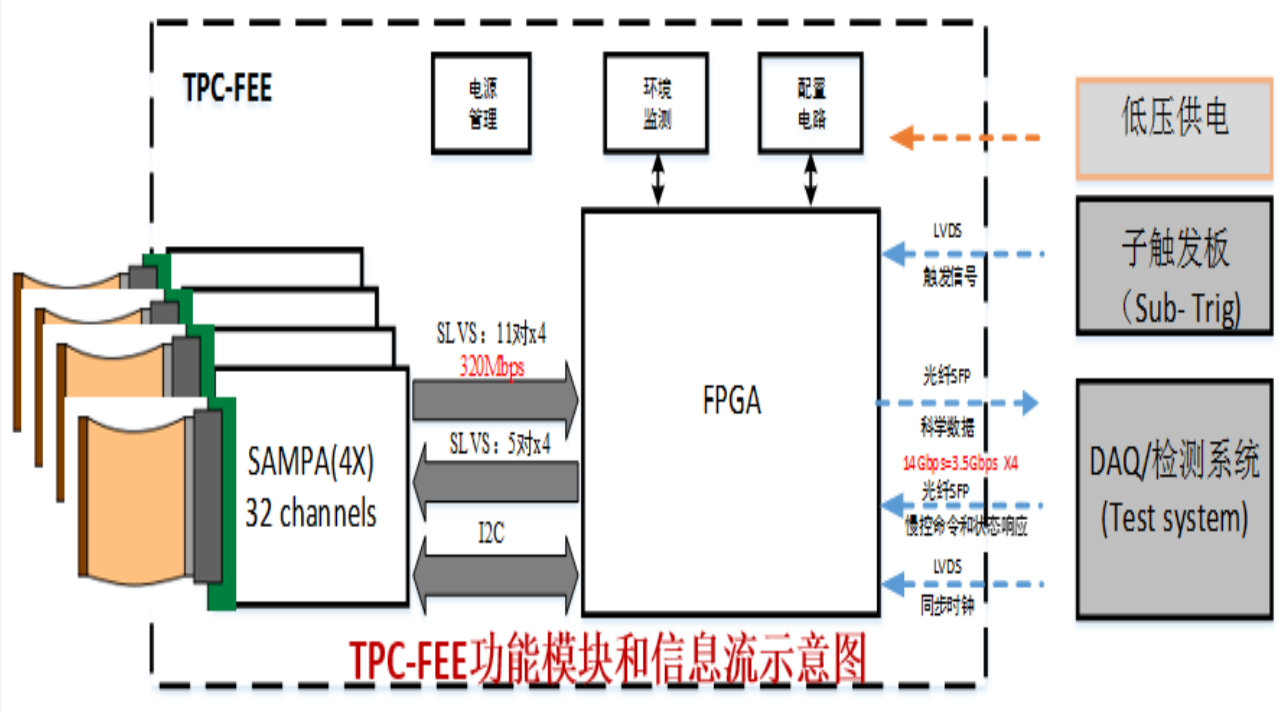
Main performance Indexes:

- Event rate : 50 kHz , 32 channels per SAMPA chip , CSA, Shaper, ADC, DSP per channel
- triggered mode & continuous mode , power consumption : less than 15 mW/ch

SAMPA electronics for CEE-TPC

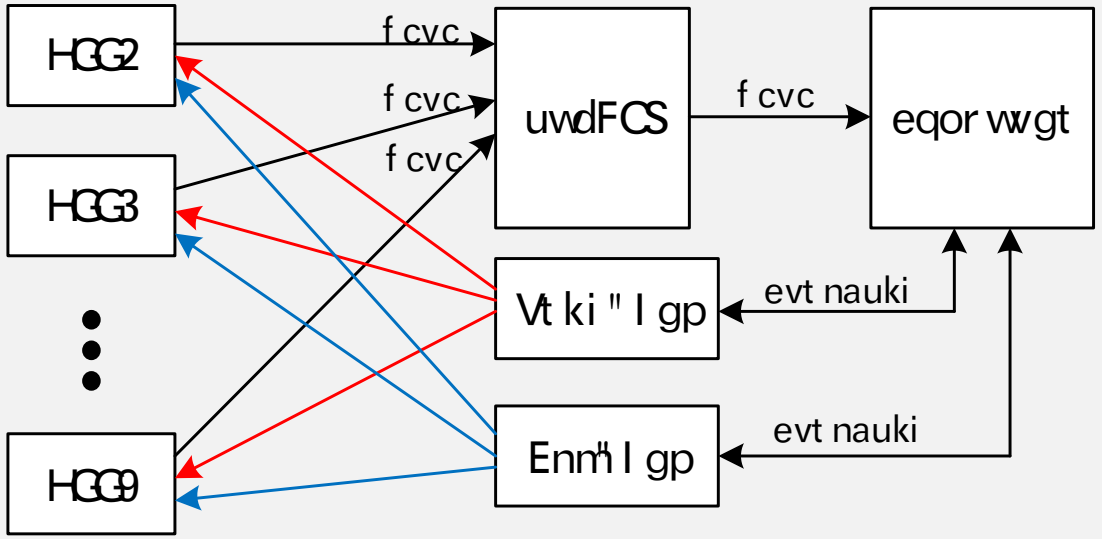
◆The diagram of electronics for CEE-TPC

Technical solution: 4 SAMPA+FPGA per FEE board



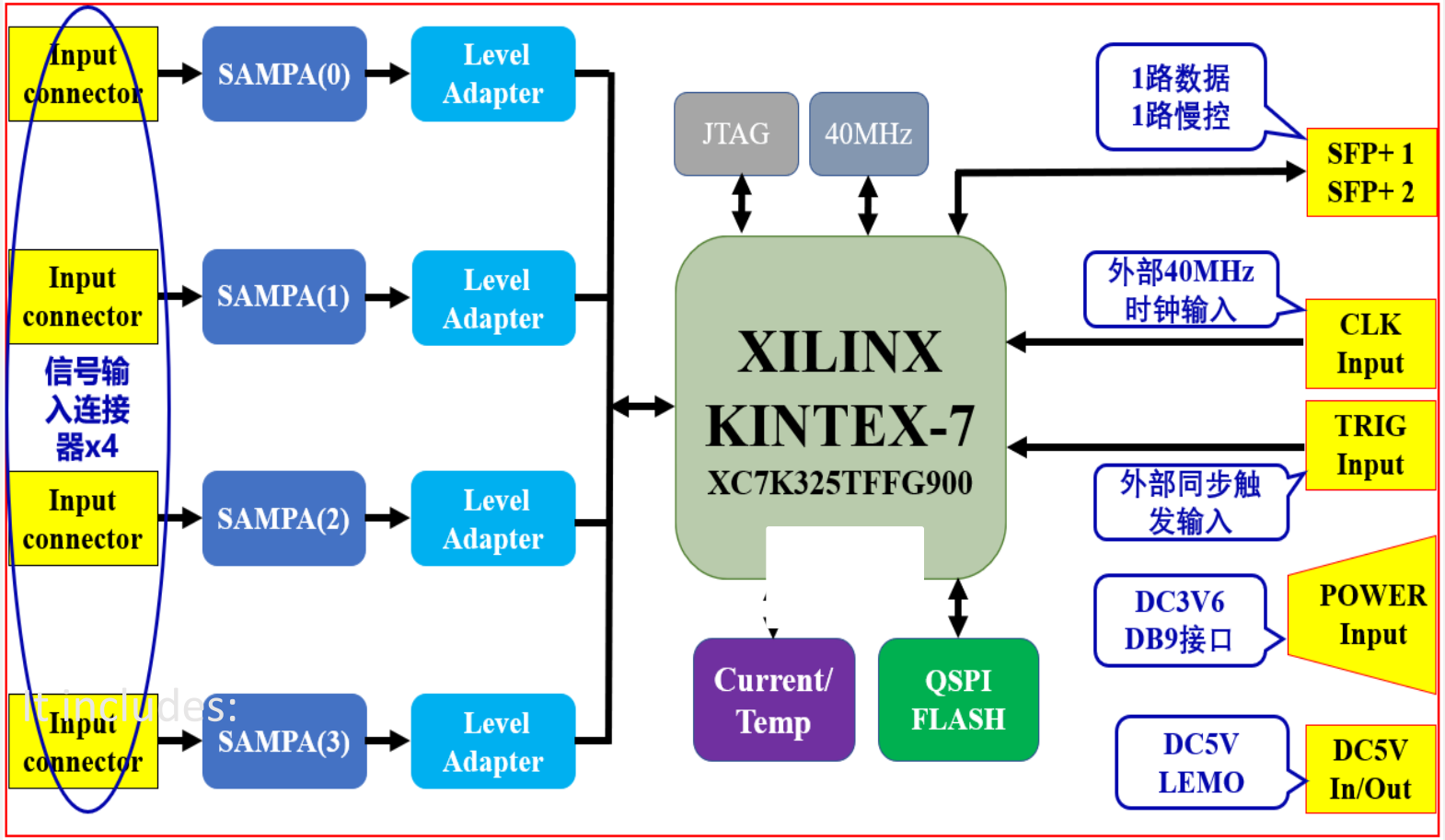
The block diagram of the FEE

The block diagram of 1024-channel TPC readout system



- The Trig Gen module provides global trigger signals and fans out to all FEEs.
- The clk Gen module provides a global clock with a frequency of 40Mhz and fans out to all FEEs.

The design of electronics for CEE-TPC



Hardware structure of TPC-FEE

Main Functions of FPGA:

- Configuration via IIC;
- data read, processing and transmission via SFP;
- On-board temperature & current monitor
- Auto power-off protection for Sampa chips

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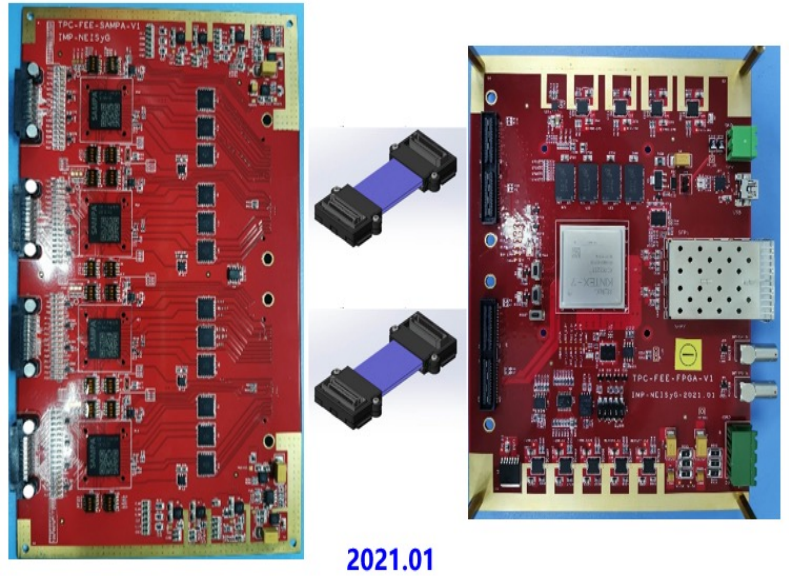
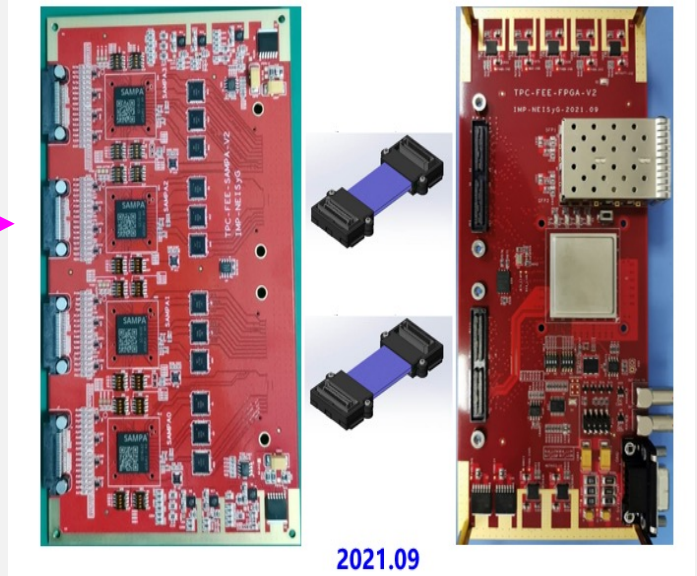
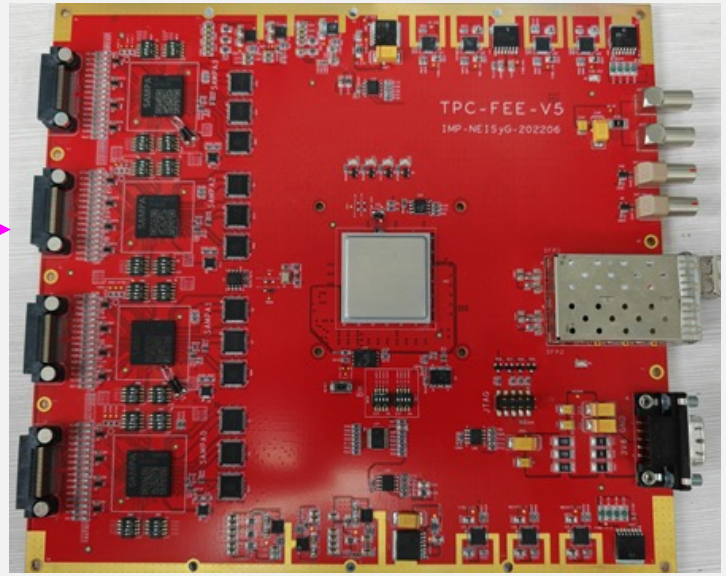
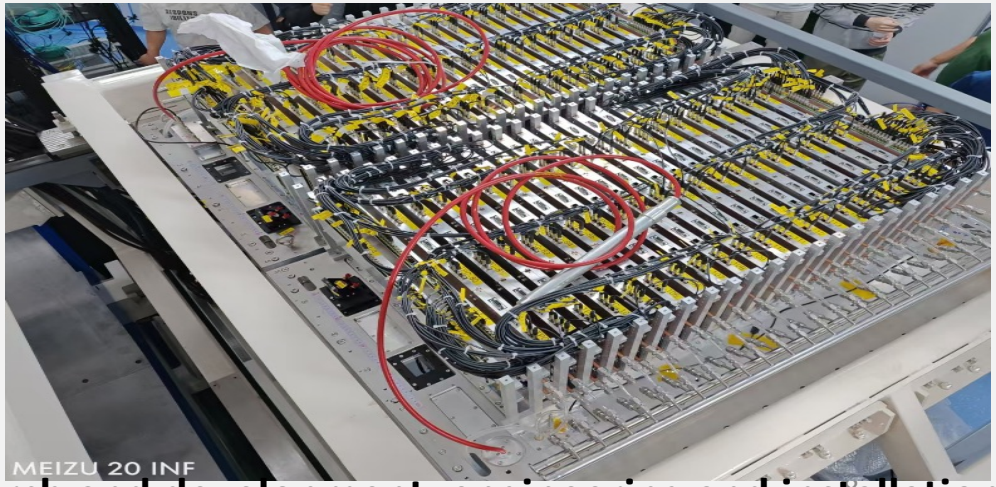
Hardware design





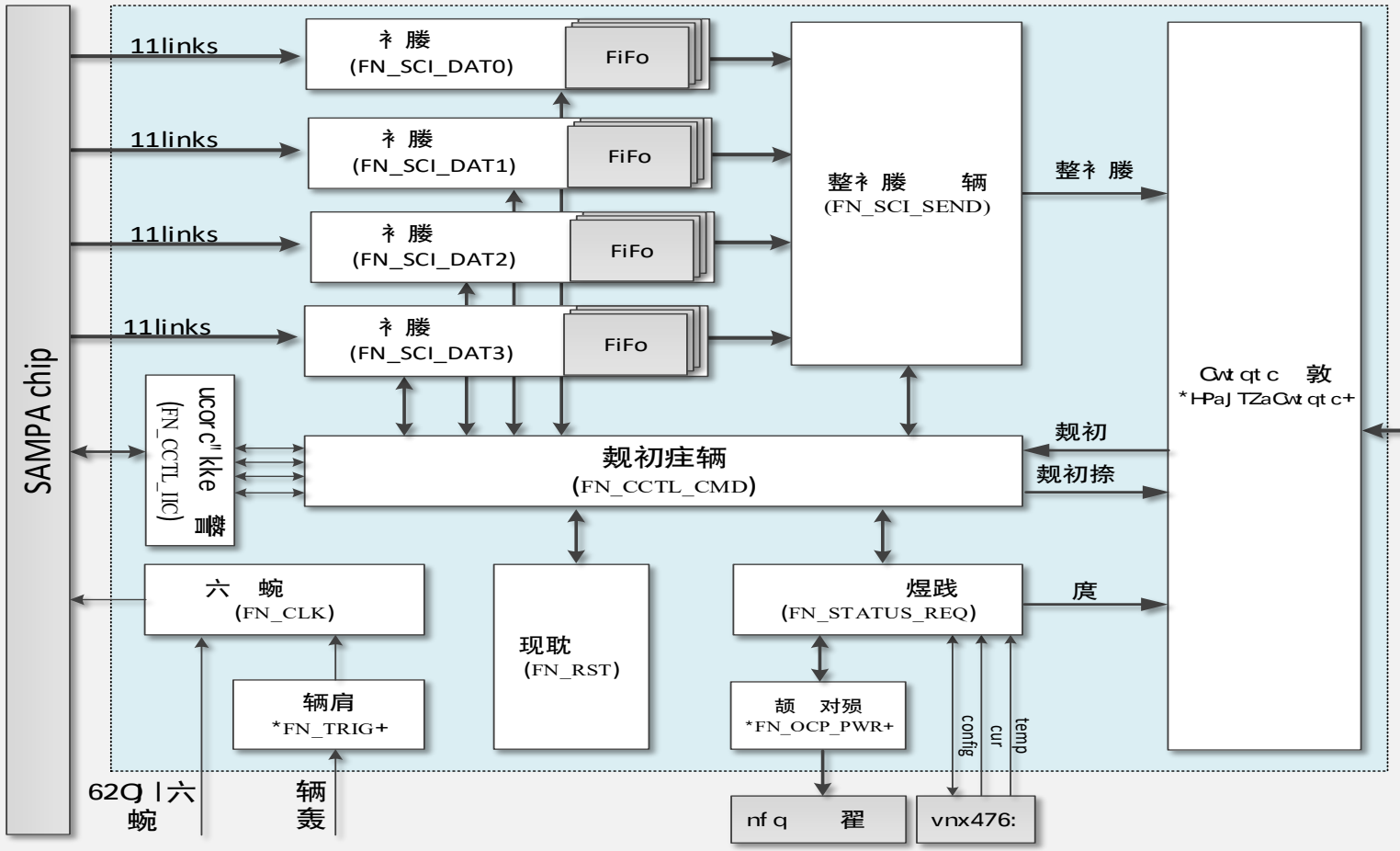


It has gone through four editions of design, In 2023, the Fourth version was completed



in 2024 The batch production is completed, in 2025Completed the research and development, engineering and installation testing of the 15,000-channel FEE engineering machine

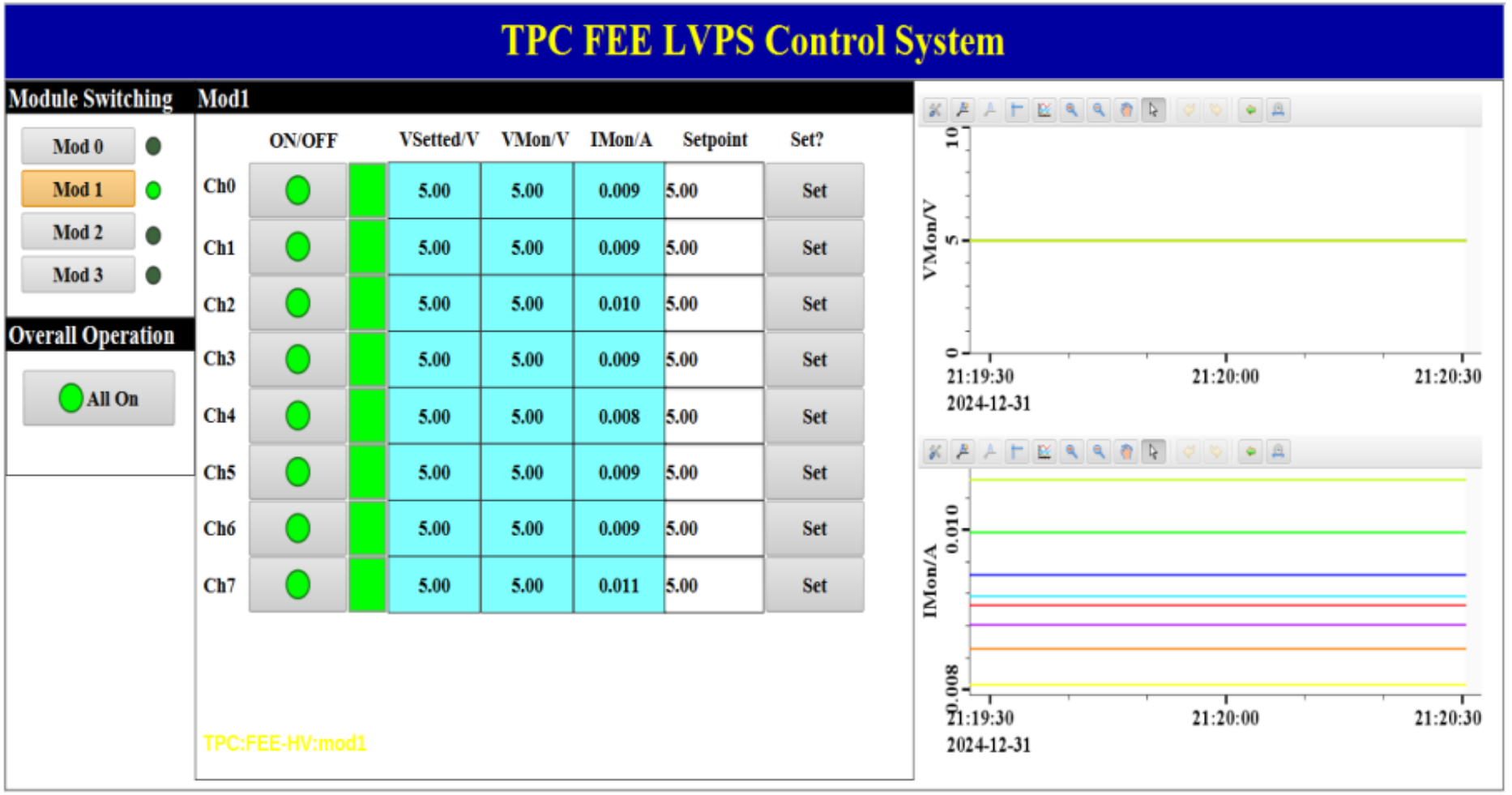
◆ Firmware structure of TPC-FEE



Task requirements:

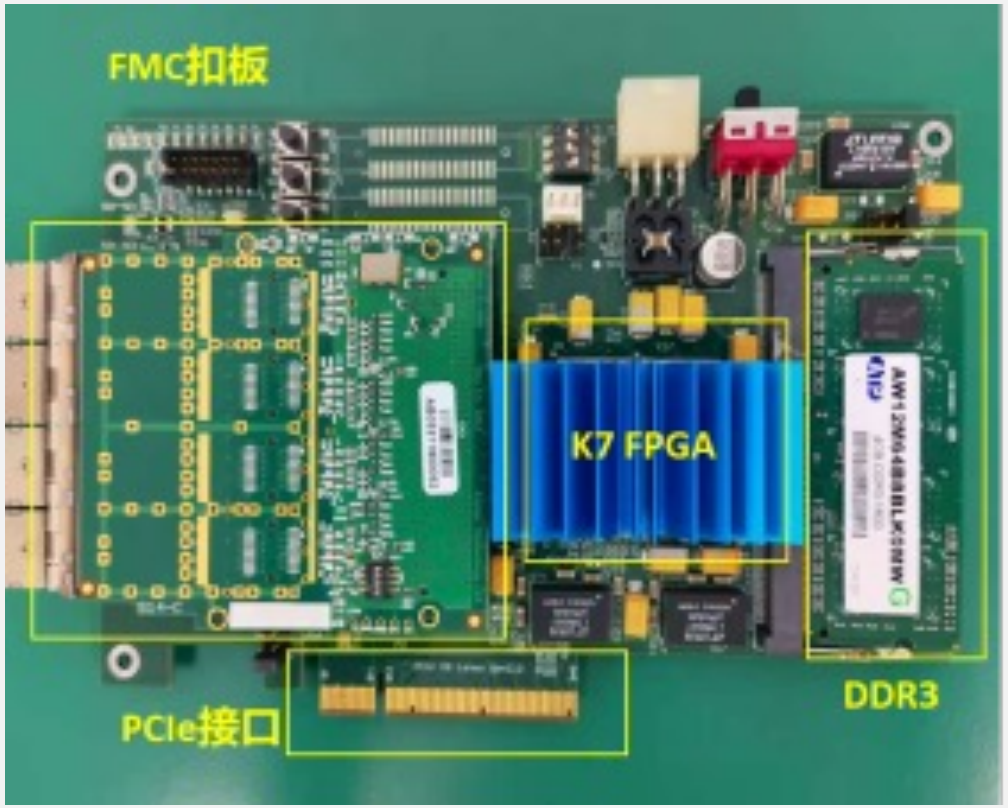
- Parameter config and control
- Scientific data reading and secondary packaging & sending
- data transceiver interface SFP
- Status telemetry,Auto Power-off Ctrl

voltage control system: Low voltage: for FEEs

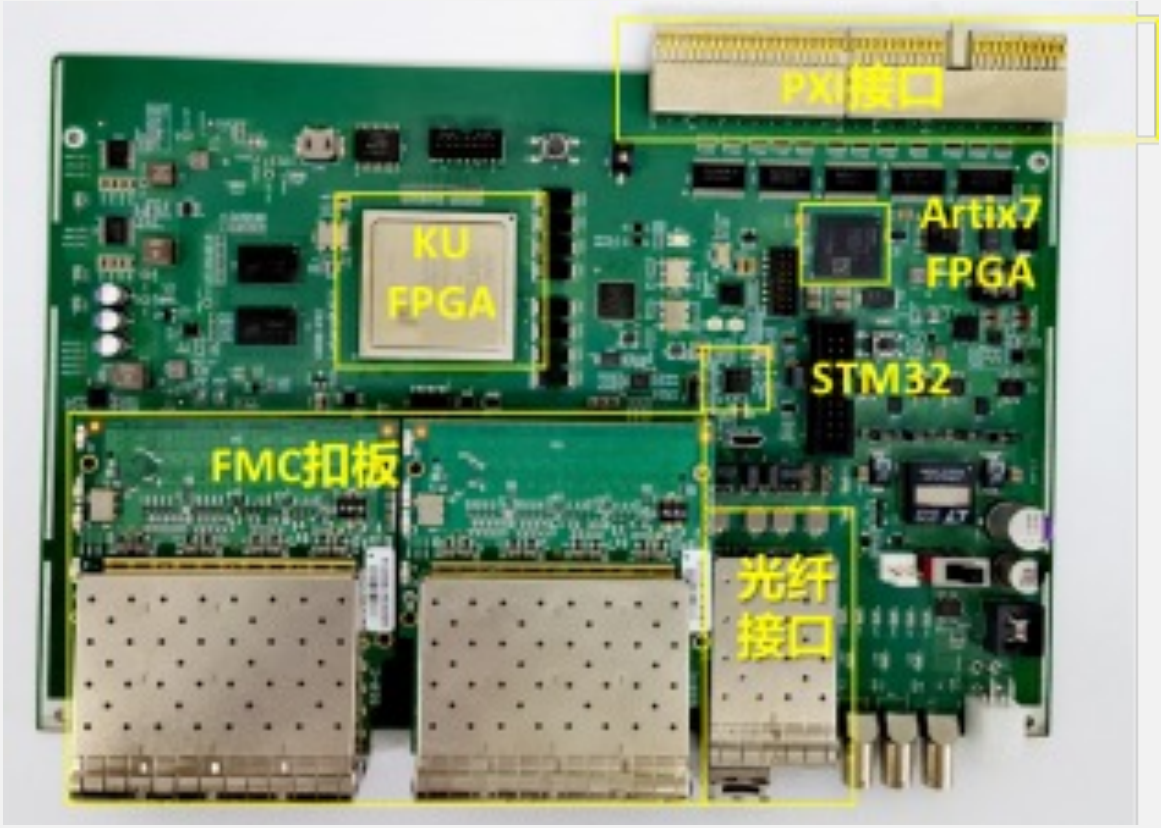


DAQ board

Main functions: To achieve the correct collection, processing, assembly, transmission and storage of scientific data



Pxi board



PCIe3.0 x8

Testing

Baseline noise test of FEE in Laboratory

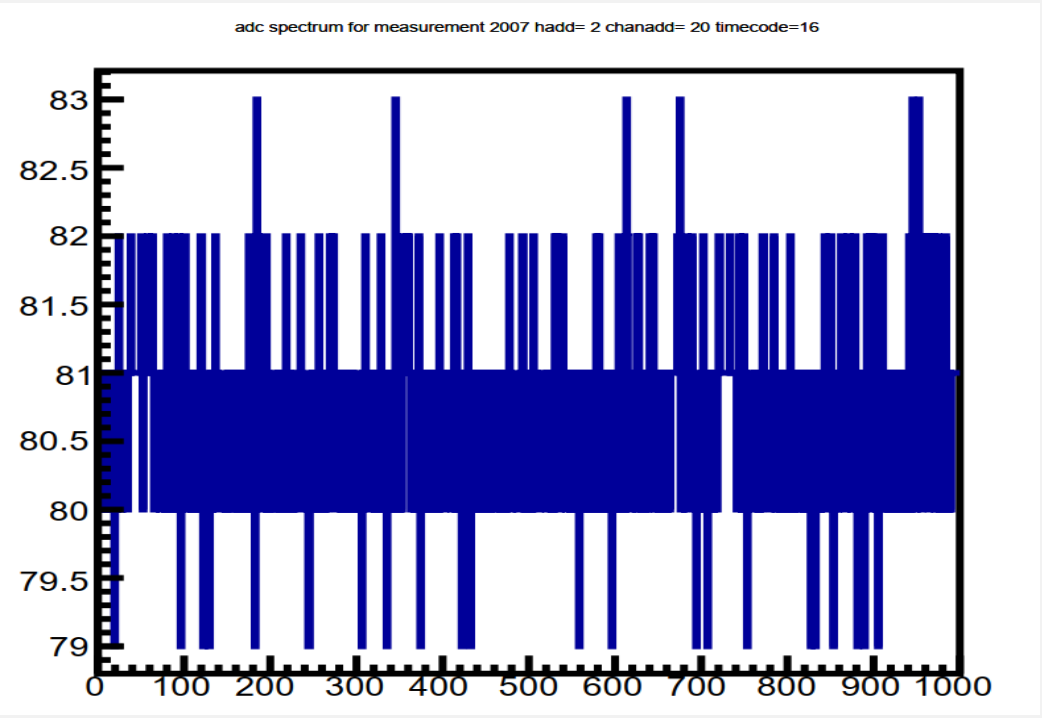


Photo of Baseline noise

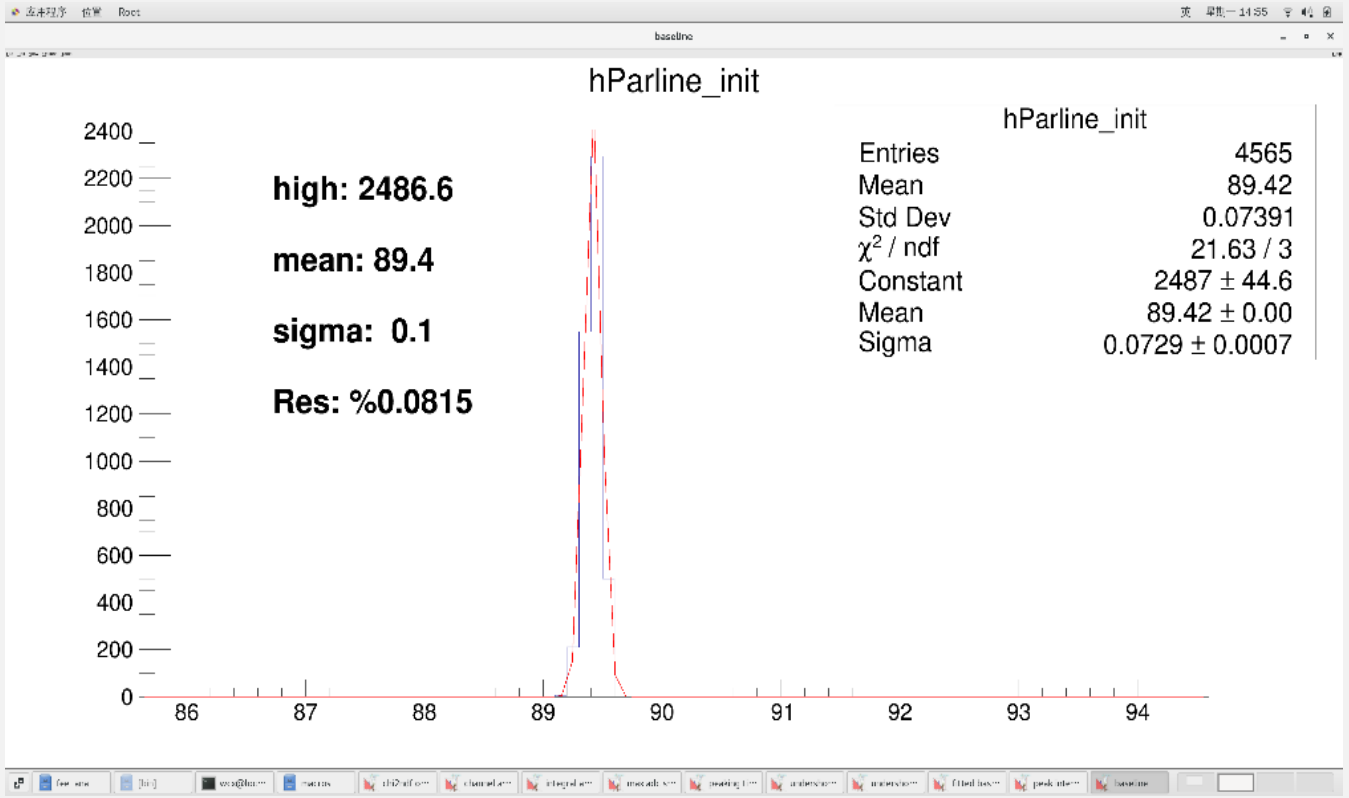
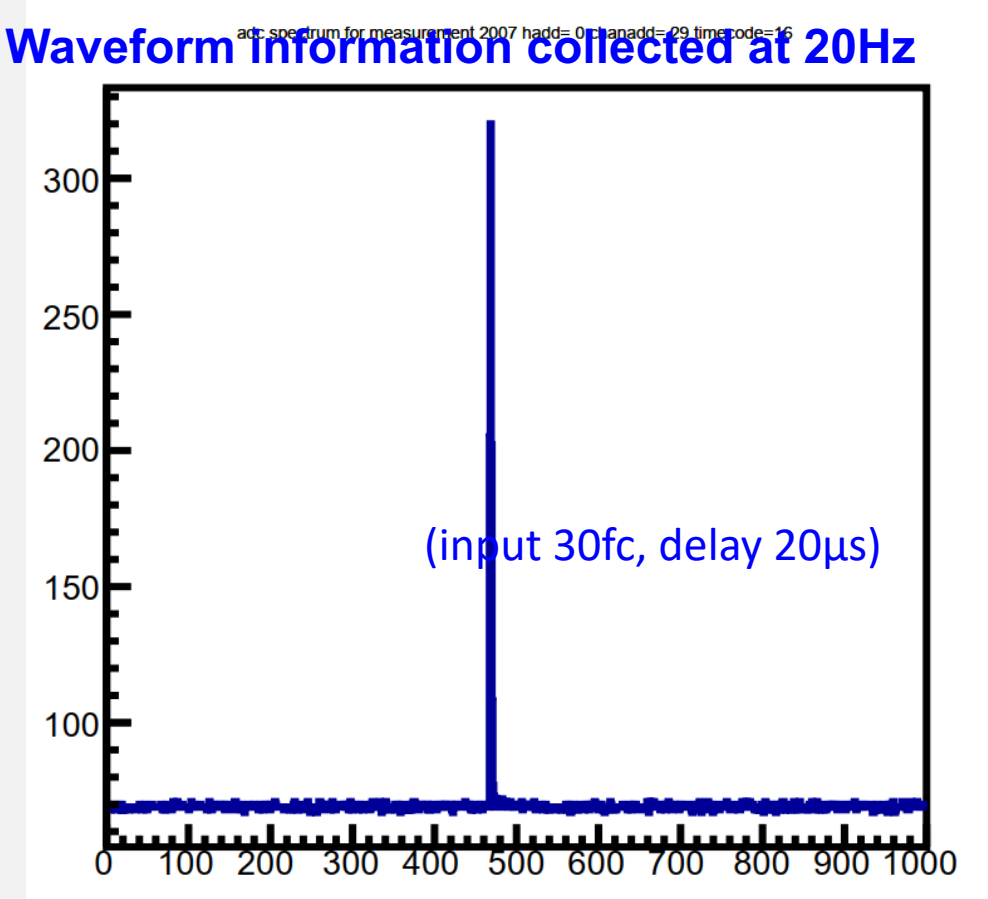


Photo of baseline noise resolution

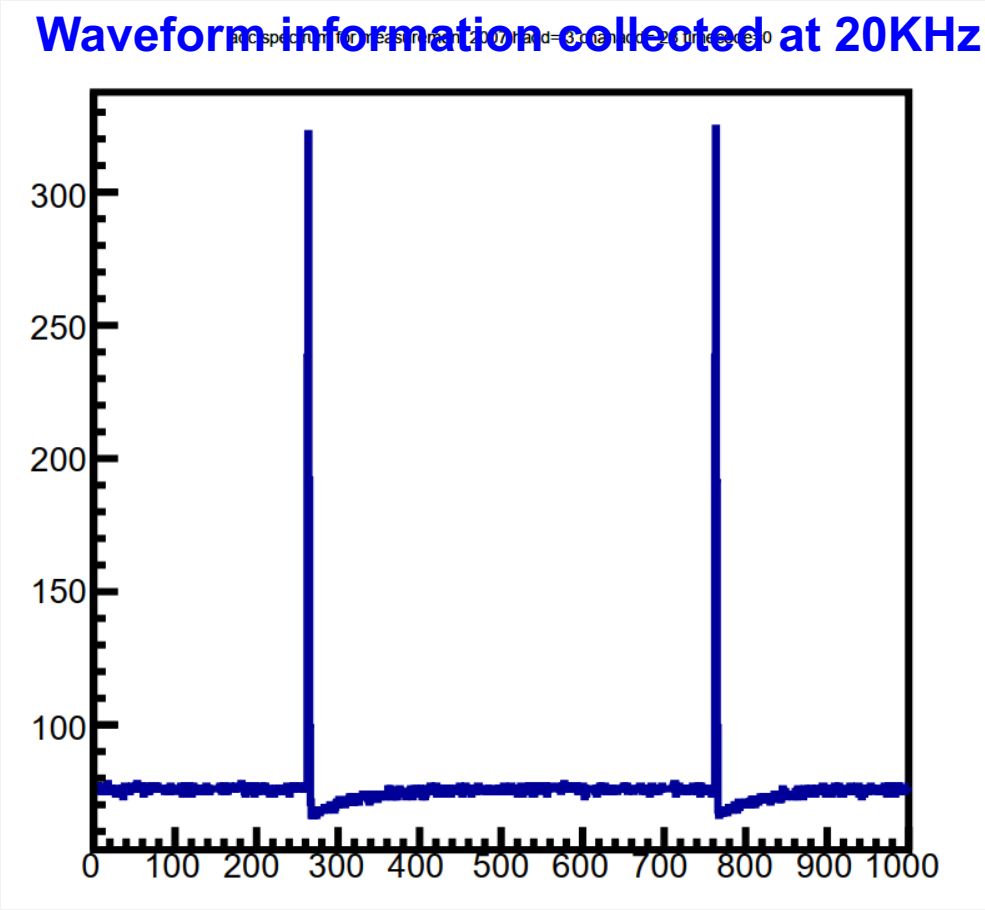
Test conclusion: The sigma of baseline noise of 128 channel is <1ADC LSB(0.1fc), equal to 625e.

The output test with different frequency input signal

Waveform information collected at 20Hz



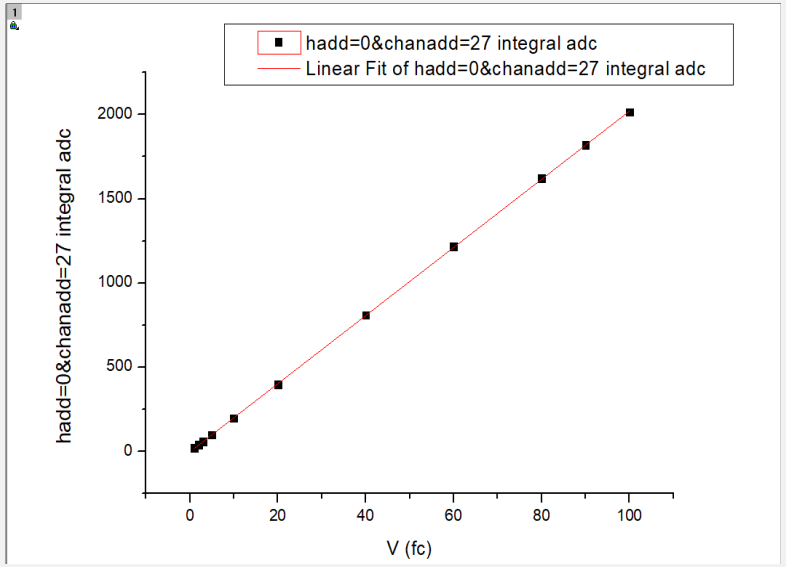
Waveform information collected at 20KHz



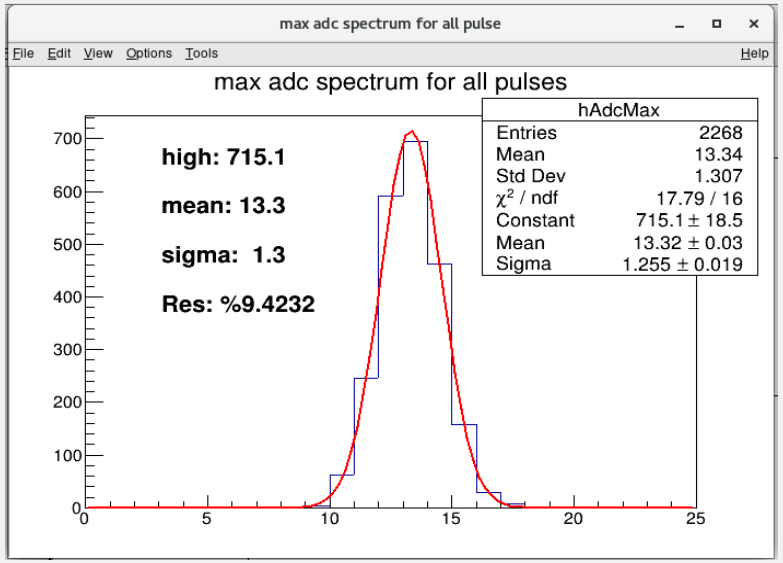
Test conclusion: TPC-FEE can respond to the input signal rate of 1Hz~20KHz, and the output amplitude meets the expectation.

Linearity and energy resolution test of TPC-FEE in Laboratory

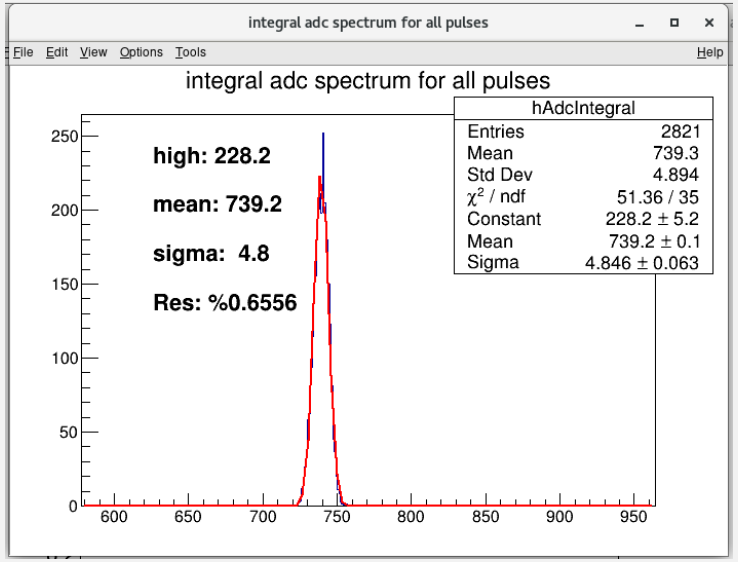
Integrate the linear error of the ADC



Output energy spectrum @ (1.4fC) input

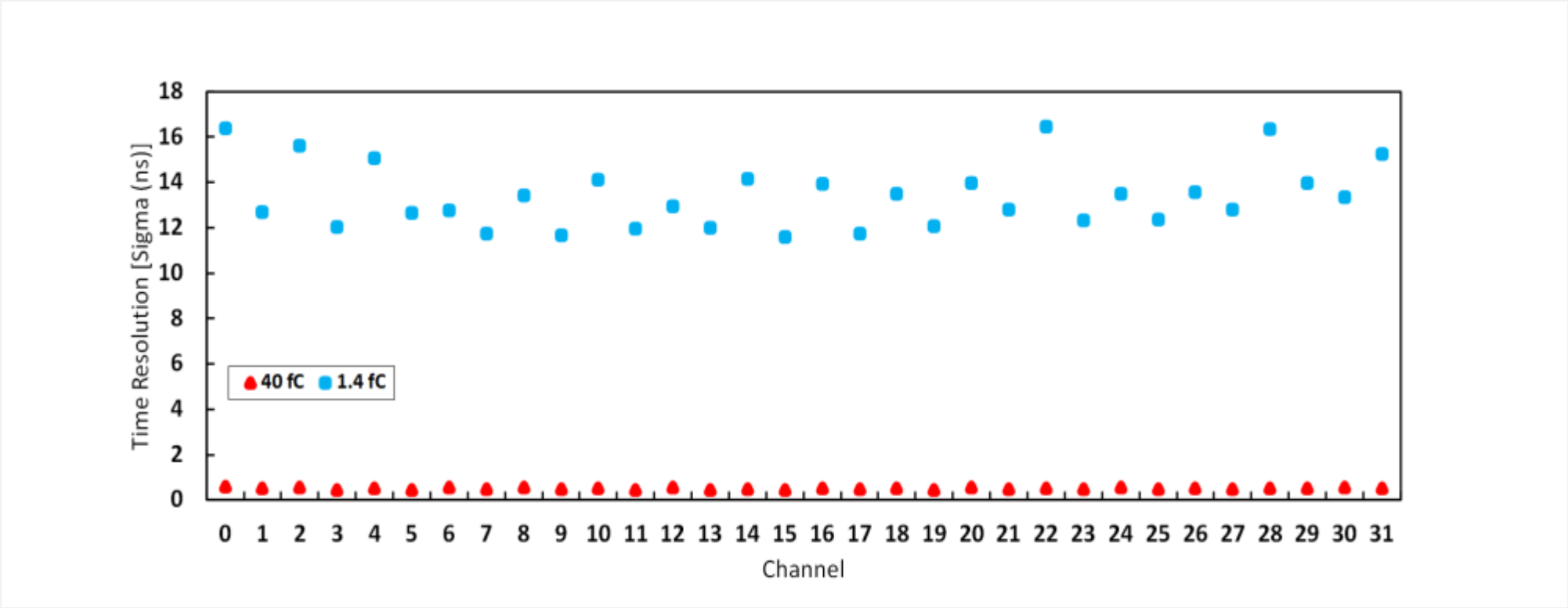


Output energyspecrum@40fC input

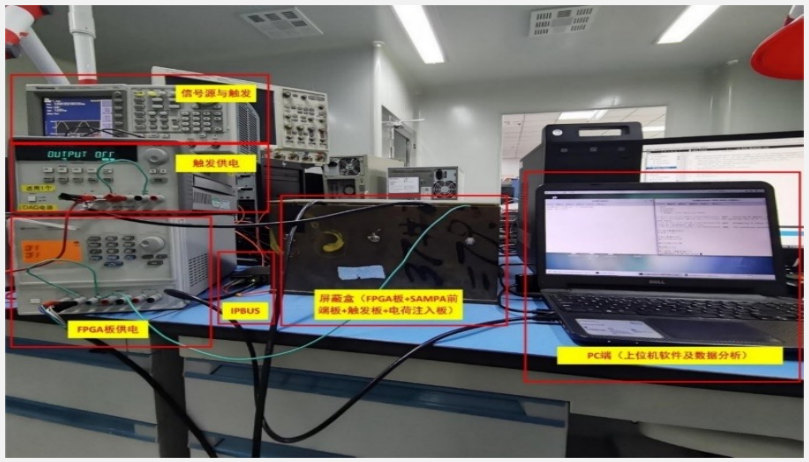


Test results: The nonlinear error of integral ADC in 1-100fc is less than 0.29%, and the nonlinear error of max ADC is less than 0.45%; The energy resolution (σ) at the minimum input charge 1.4 fC is better than 10%.

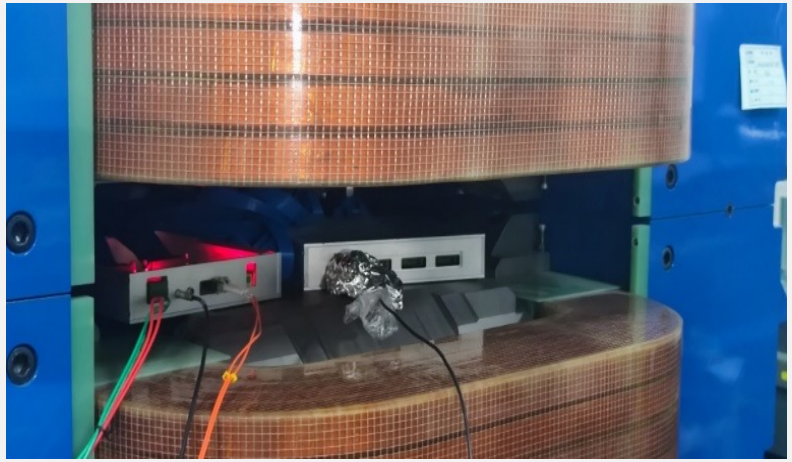
The time resolution test of TPC-FEE in Laboratory



The time resolution (sigma) of 32 channels in one SAMPAs in FEE at 1.4 fC and 40 fC input charge signal

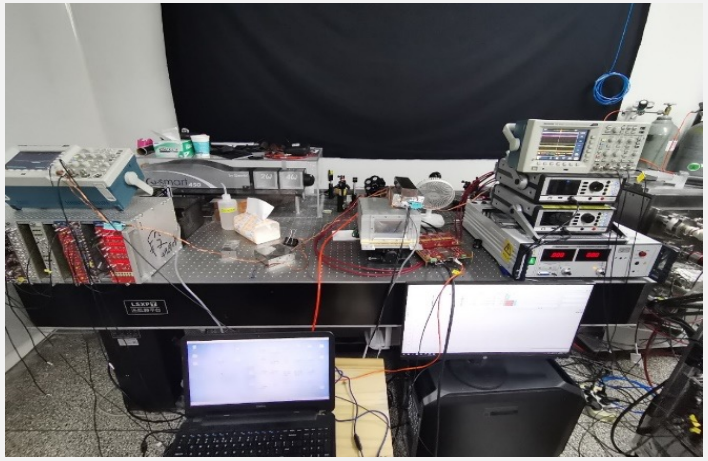


Laboratory FEE test

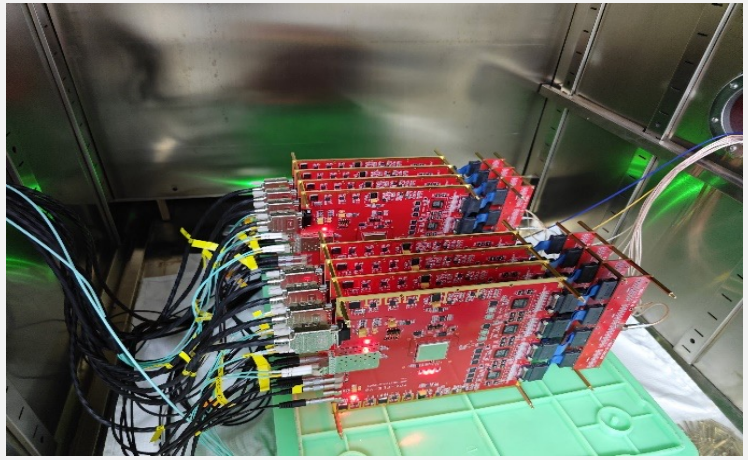


High magnetic field environment test

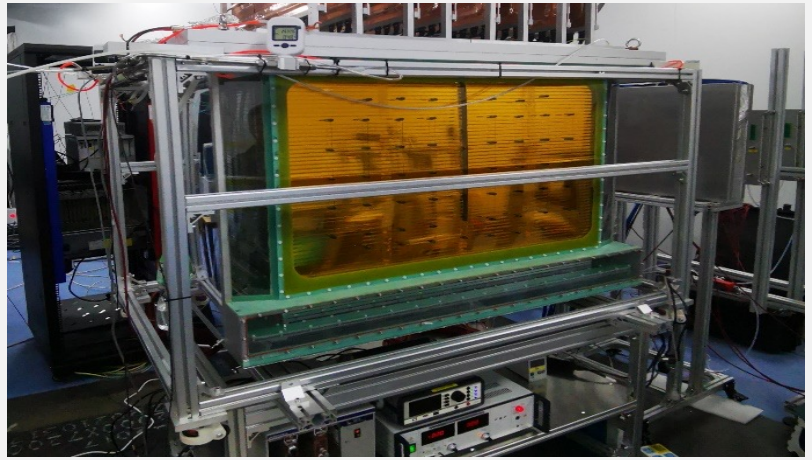
Laboratory FEE with detector test



Laser calibration test

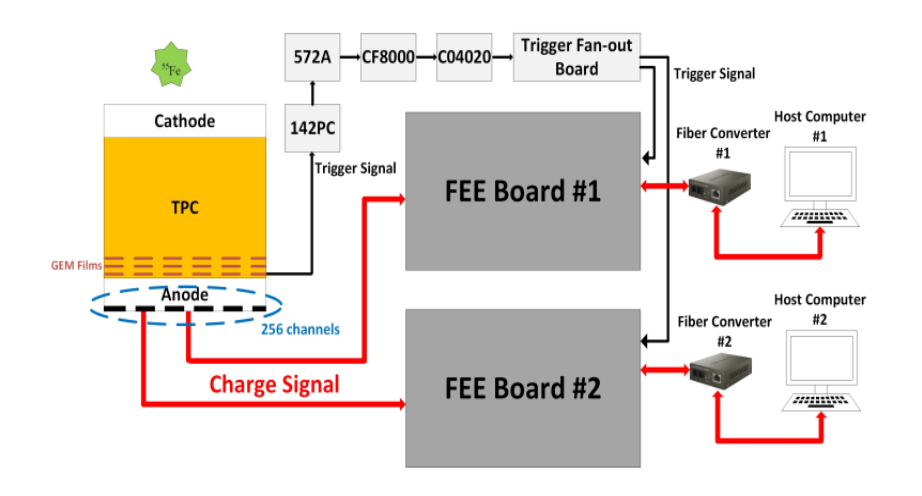


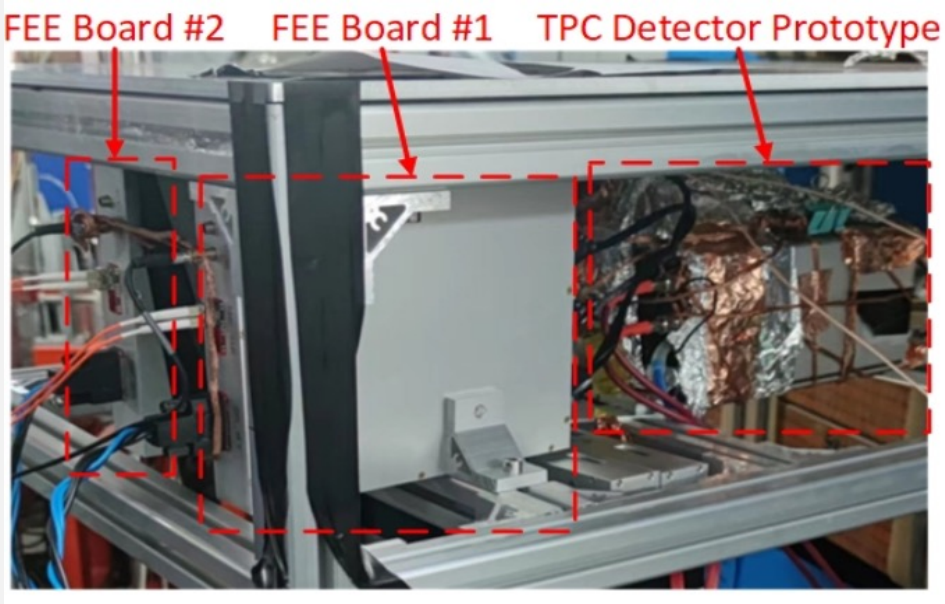
Large scale temperature environment test

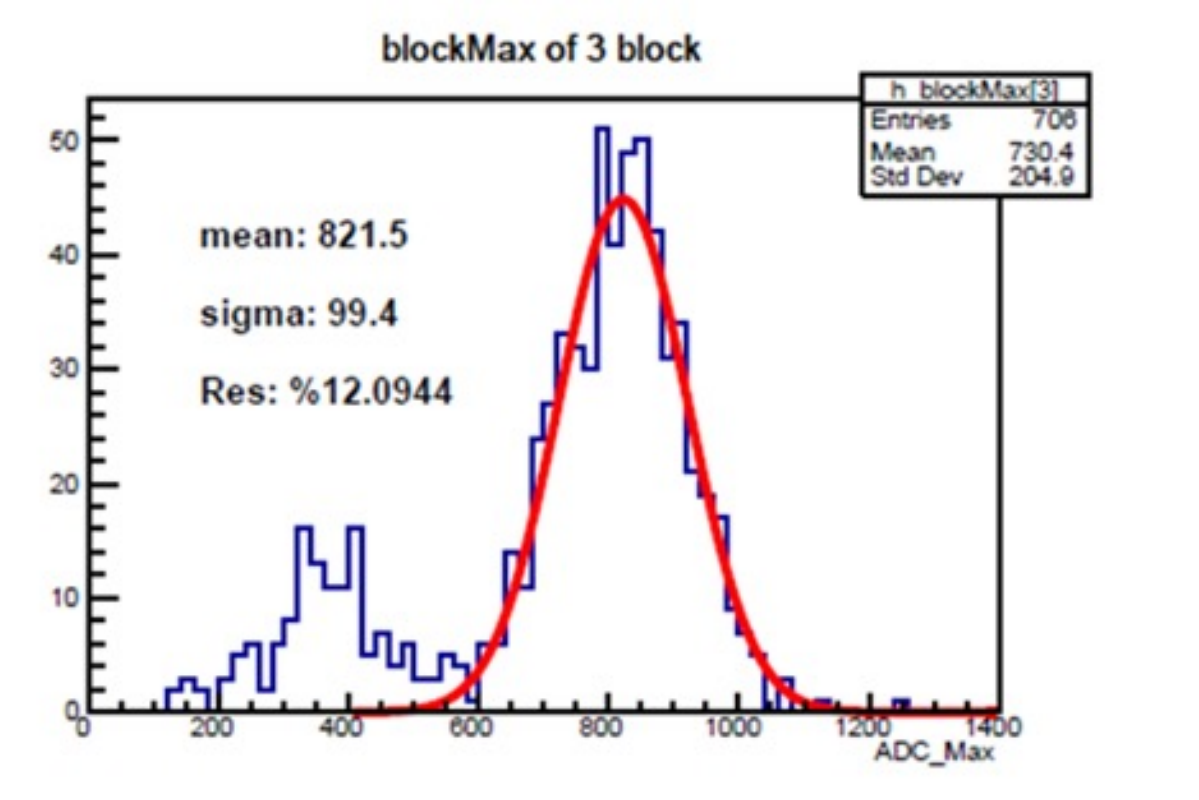


Beam test

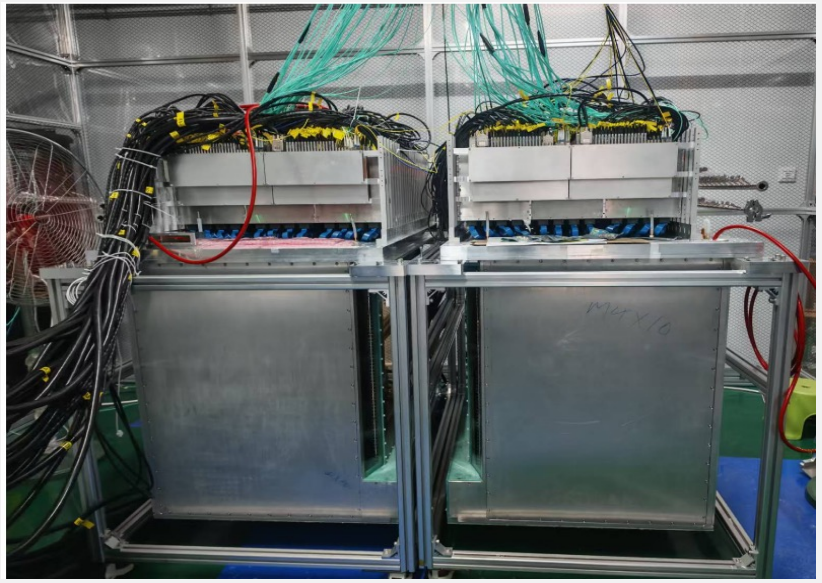
FEE & Detector test: Iron source (^{55}Fe)

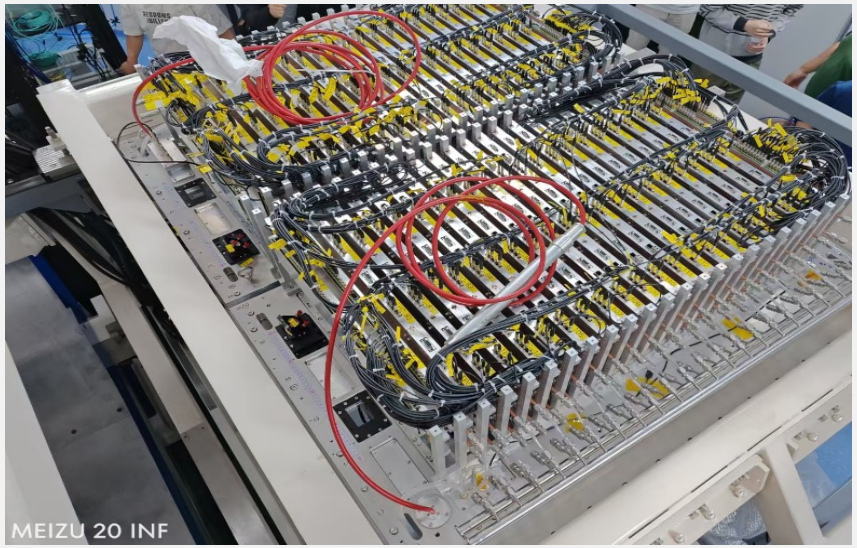


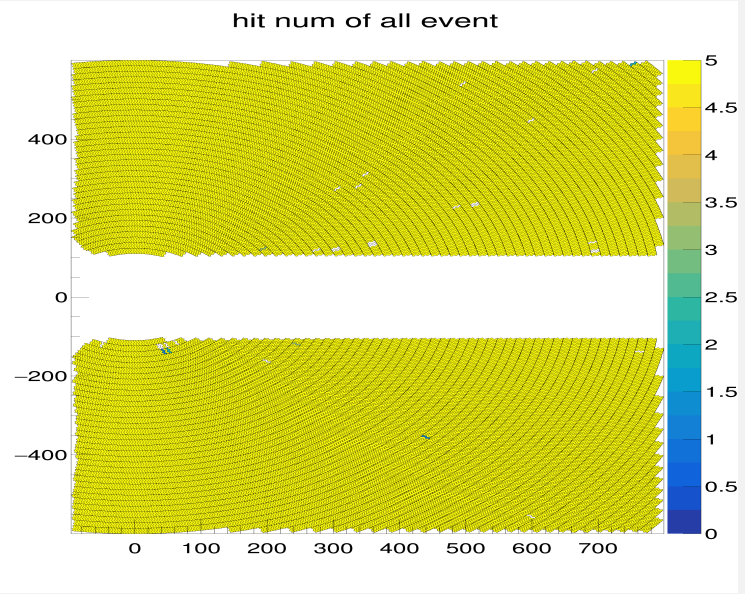


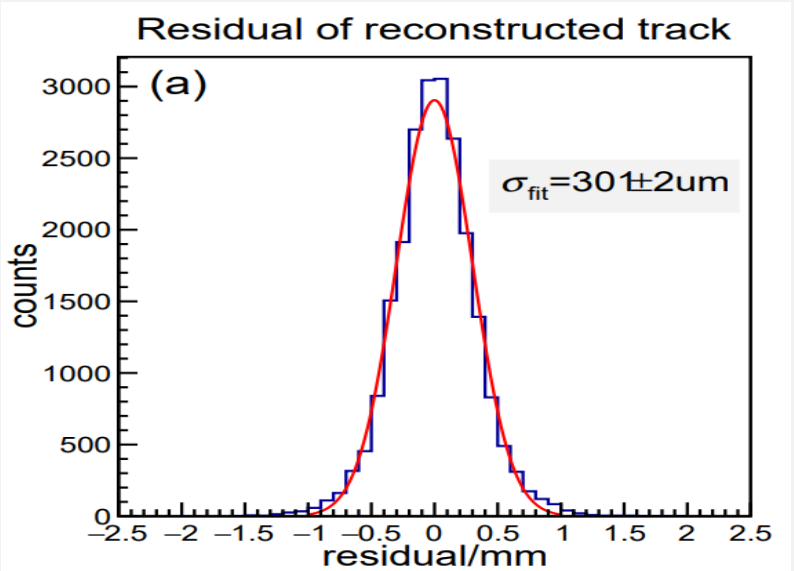


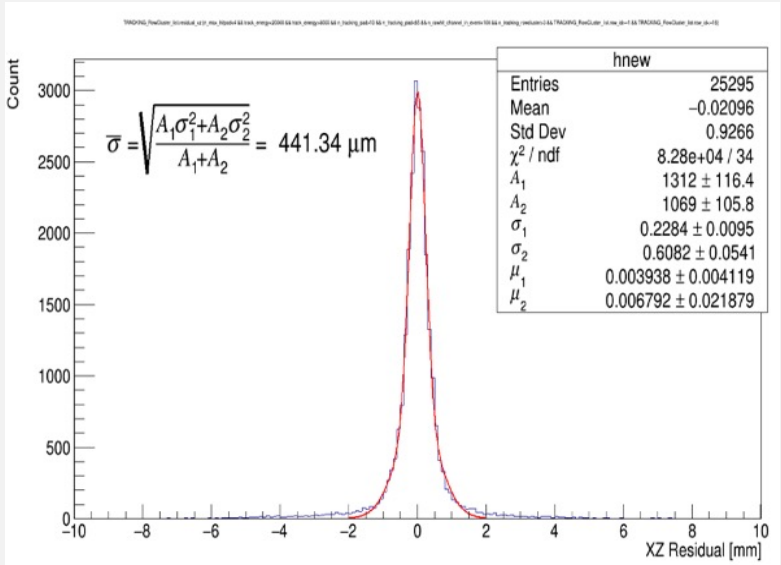
Partial block energy spectrum without edge effects and dead channels (res=sigma/mean)

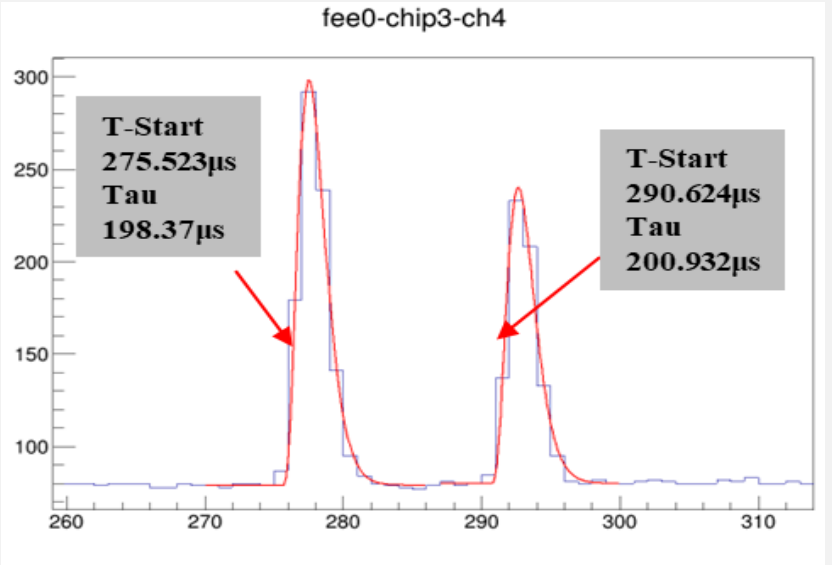



MEIZU 20 INF


hit num of all event
400
200
0
−200
−400
0
100
200
300
400
500
600
700
5
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0


Residual of reconstructed track
(a)
σ_{fit}=301±2um
counts
residual/mm
3000
2500
2000
1500
1000
500
0
−2.5
−2
−1.5
−1
−0.5
0
0.5
1
1.5
2
2.5


$\overline{\sigma} = \sqrt{\frac{A_1\sigma_1^2+A_2\sigma_2^2}{A_1+A_2}}$ = 441.34 µm
hnew
Entries 25295
Mean −0.02096
Std Dev 0.9266
χ^2 / ndf 8.28e+04 / 34
A_1 1312 ± 116.4
A_2 1069 ± 105.8
σ_1 0.2284 ± 0.0095
σ_2 0.6082 ± 0.0541
μ_1 0.003938 ± 0.004119
μ_2 0.006792 ± 0.021879
Count
XZ Residual [mm]


fee0-chip3-ch4
T-Start
275.523µs
Tau
198.37µs
T-Start
290.624µs
Tau
200.932µs

Summary

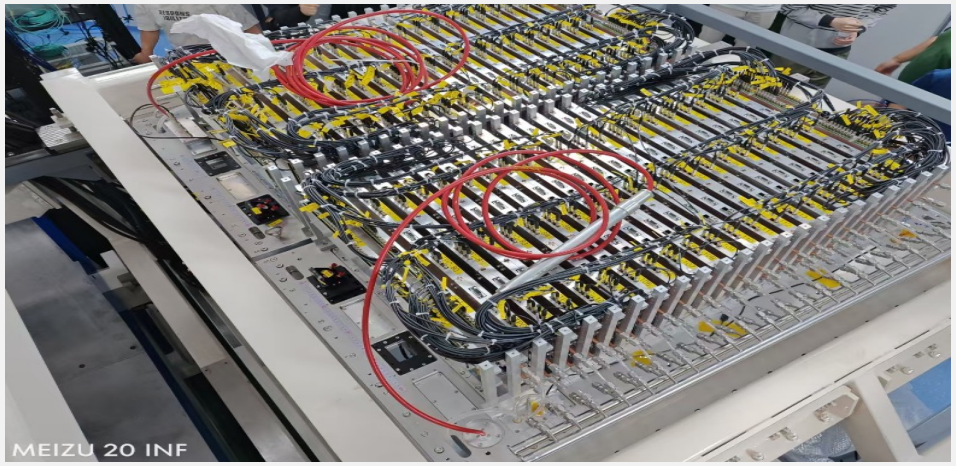
- **A multichannel readout electronics (128 channels/ board) has been developed for CEE –TPC**
  - low noise, and high-speed FEE, with a readout system of 15,000 channels
  - high case rates : adopting an advanced stream processing method and a 10-gigabit optical fiber readout architecture

- **The test results show that the TPC electronics meet the noise, dynamic range, integral nonlinearity, trigger rate and other indicators.**

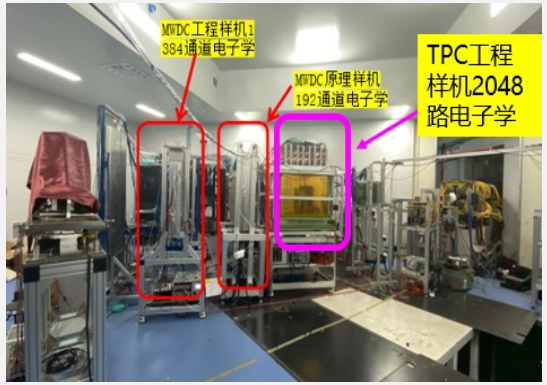
- **In 2024 The batch production is completed ,all performance testing and assemble with CEE-TPC have been finished ,and the experiment is about to start in 2025.**

Thanks!

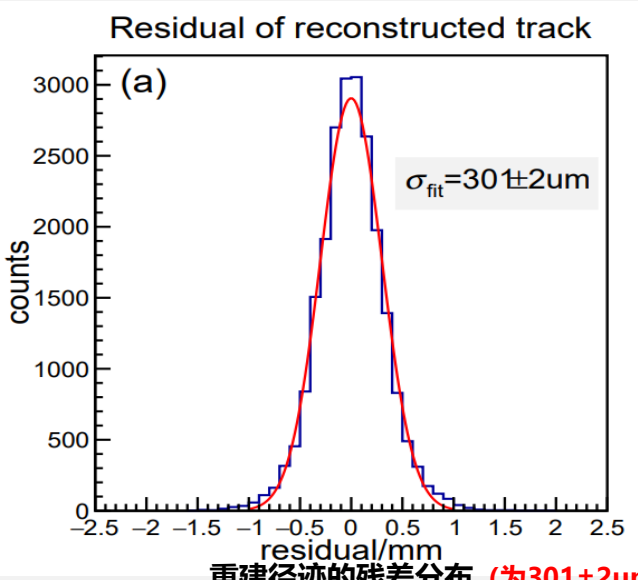
- **完成15000通道FEE工程机的研制、批产，工程化和安装测试**



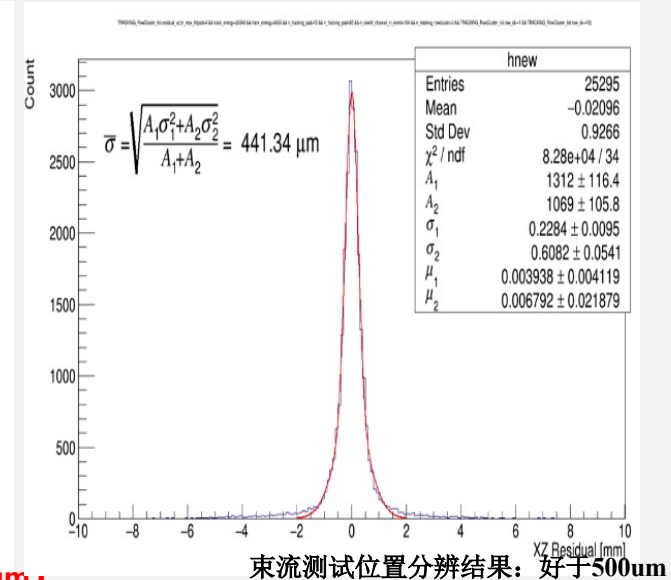
- **完成3次束流实验的验证，系统联调以及束流测试结果都满足指标，同时2025年5月通过了基金委的第1次技术验收！**



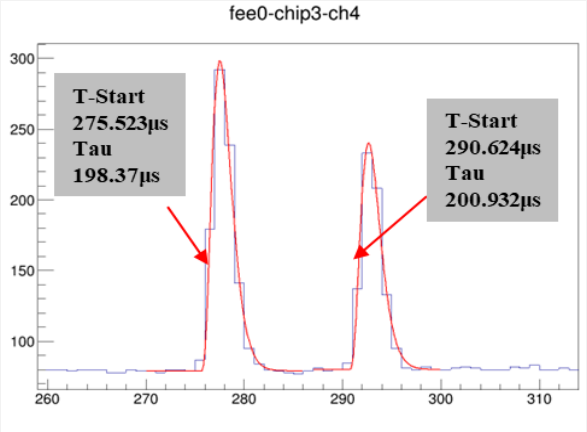
束流实现场验



重建径迹的残差分布（为301±2um）



束流测试位置分辨结果：好于500um



激光标定：双径迹分辨能力好于1cm