Status of activities of FAZIA in Korea

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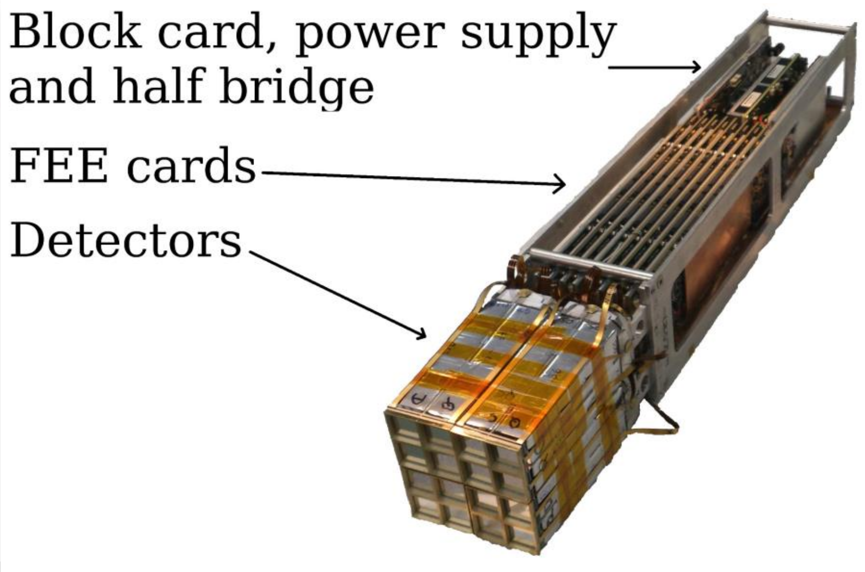
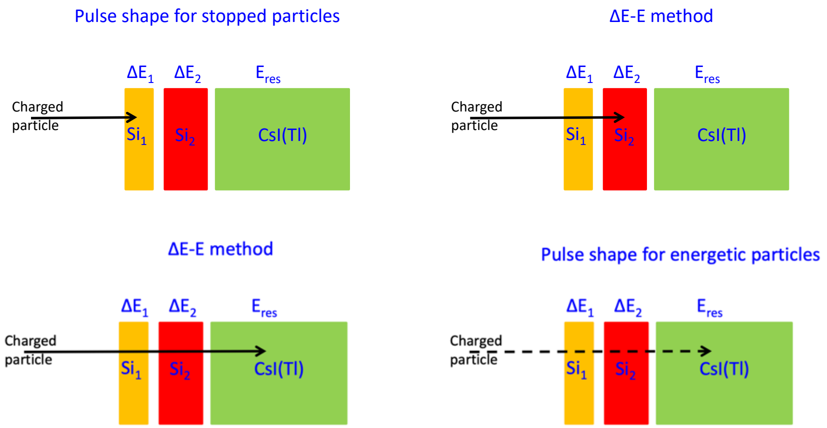
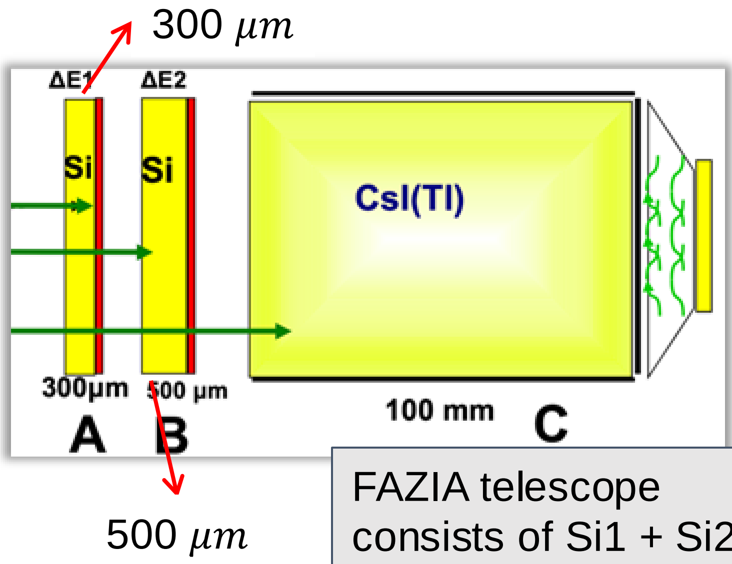
2025 CENuM Workshop
2025. 1. 19

FAZIA detector

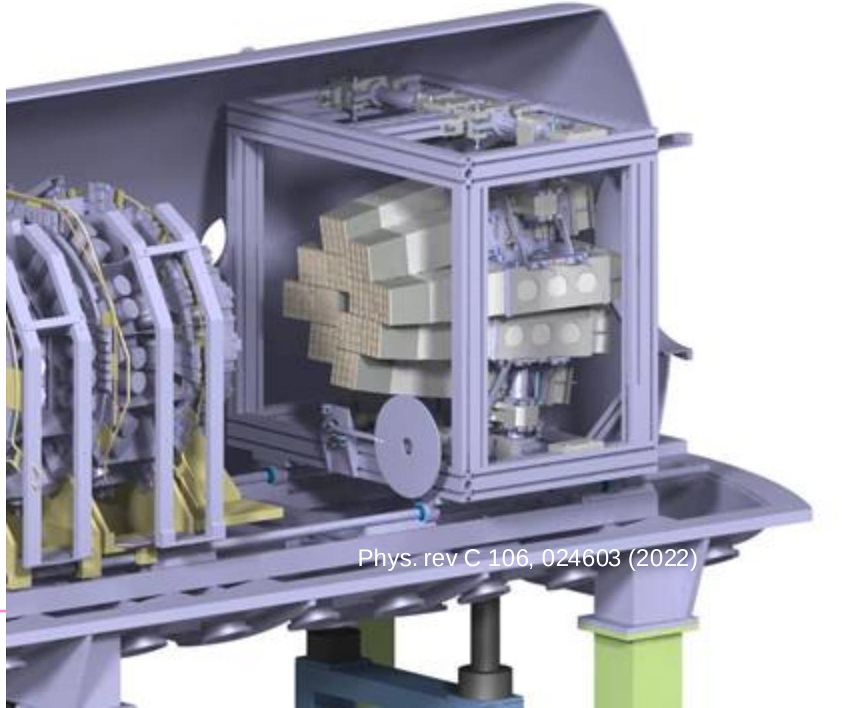


- FAZIA(Forward-angle A and Z Identification Array) detector consists of two different thickness silicon sensors and one CsI(Tl) scintillator, forming the FAZIA telescope
- Eight front-end electronics(FEE) cards are connected to the backside of the telescope
- The telescope structure allows particle identification and isotope separation through the ΔE - E method





FAZIA telescope consists of Si1 + Si2 + CsI scintillator

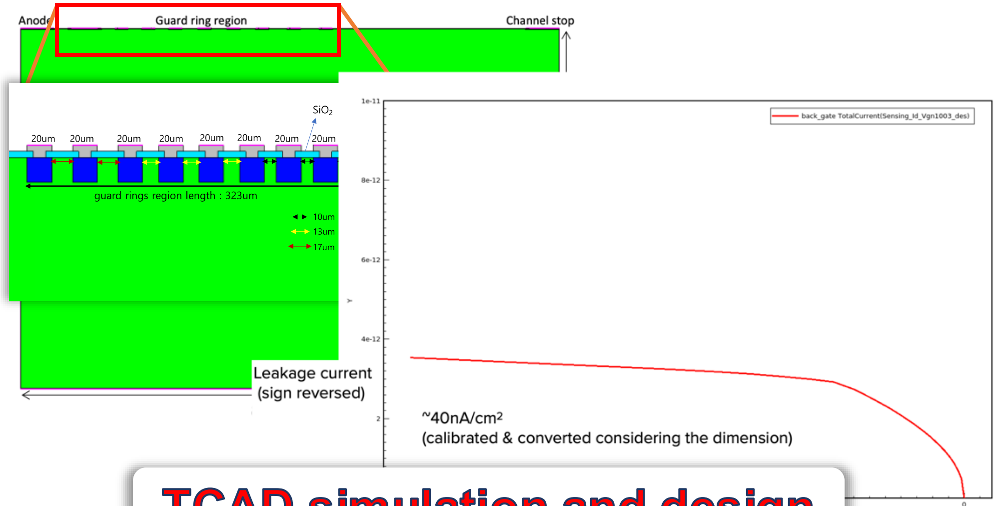


Phys. rev C 106, 024603 (2022)

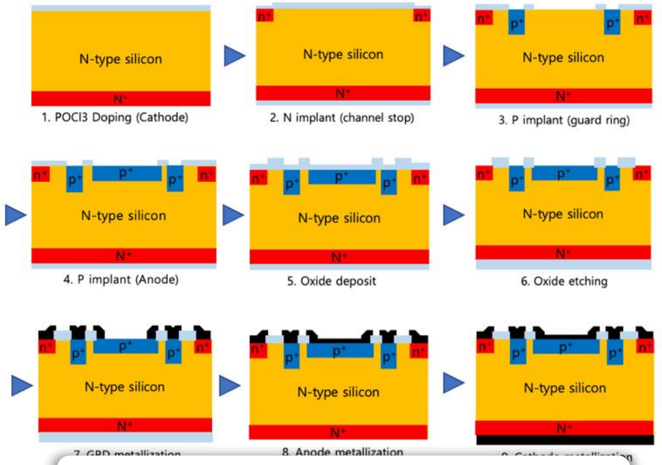
R&D for future detector upgrade

- **Upgrade**
  - Extended identification capability, better granularity
  - Flexible installation in the limited space (vacuum chamber)
  - Application of the modern technology to detectors and FEE
  - Larger acceptance: Plan to increase the number of FAZIA blocks in difference places to benefit from any opportunities to perform more comprehensive measurements
- **Sensor development** R&D Plans in Korea
  - Development of thinner and thicker silicon sensor
  - Fabrication of support modules for silicon sensors
- **Electronics development** R&D Plans in Korea
  - Development and production of a new FEE card
  - Separation of the pre-amp stage of the FEE card for chip tests

Thick(750 μm) and Thin(115 μm) Si sensor development

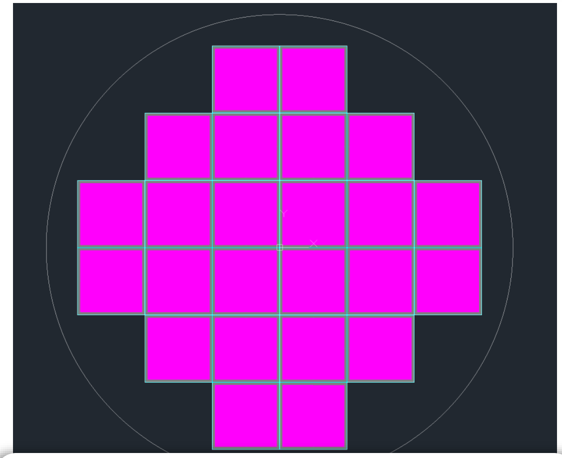


TCAD simulation and design

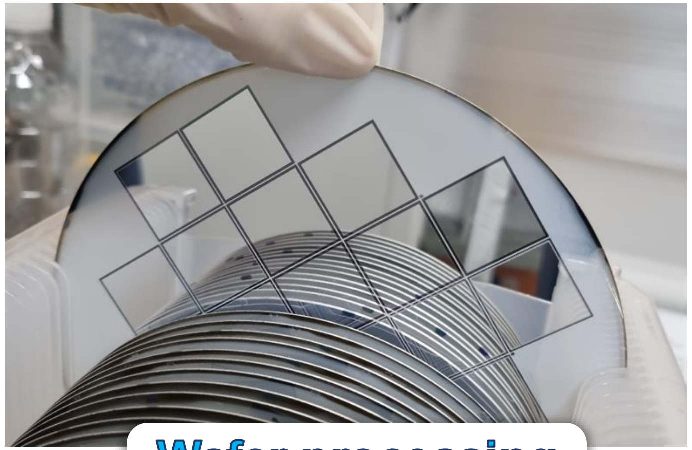


Si sensor process flow

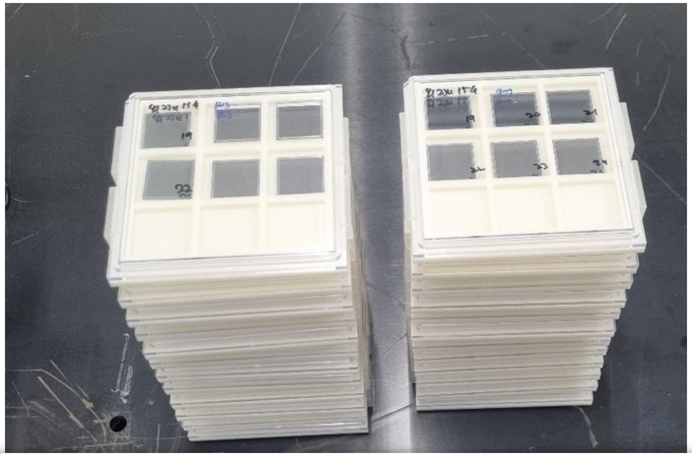
- Designing Si sensor patterns using TCAD simulation
- To optimize the design, several designs fabricated simultaneously
- Successfully produced thin and thick Si sensor (115 μm and 750 μm thickness, respectively)



Photomask production (by MicroImage)



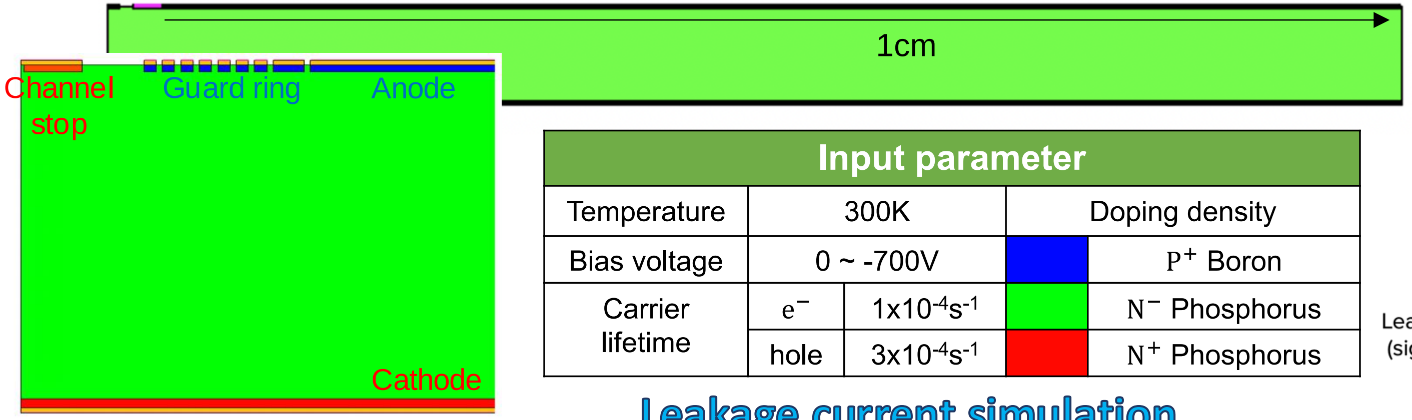
Wafer processing (by ETRI)



Thinning & dicing (by TRinnoTech, MEMSPACK)

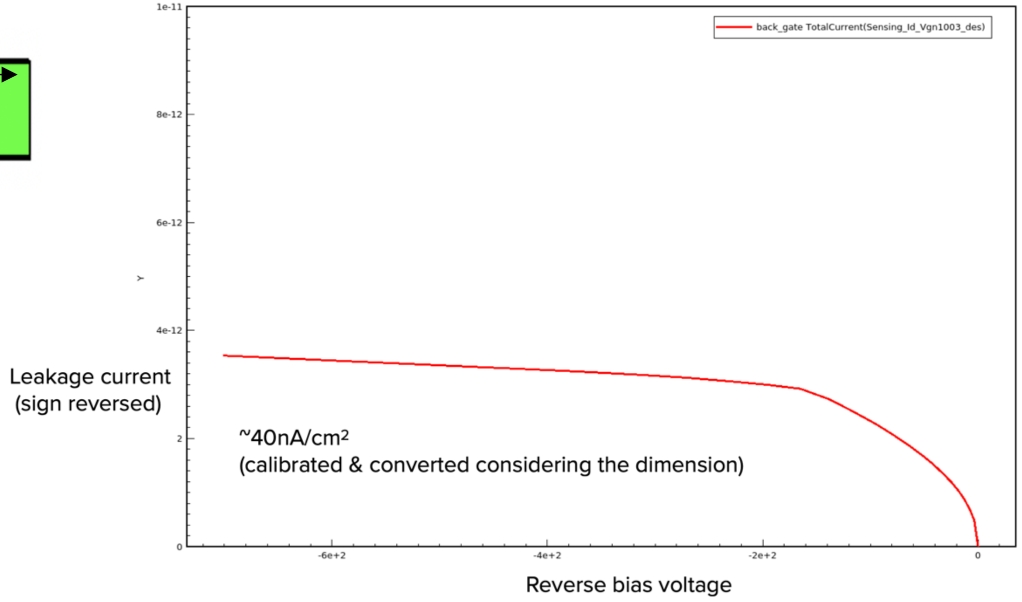
Investigation of silicon sensor using TCAD simulation

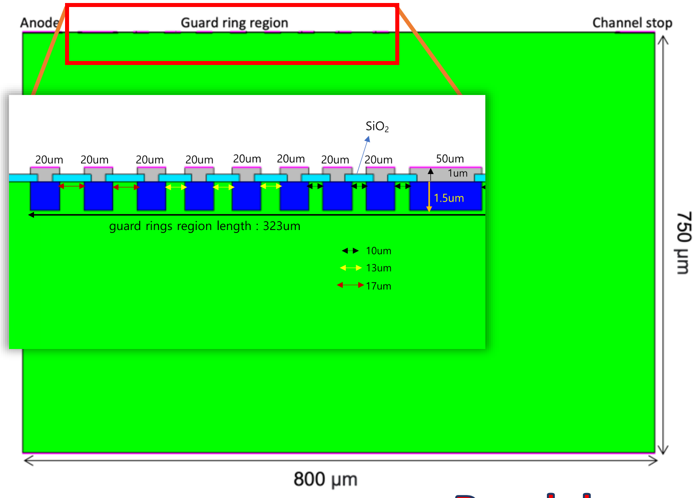
Half of cross section of 2 x 2 cm^2 chip



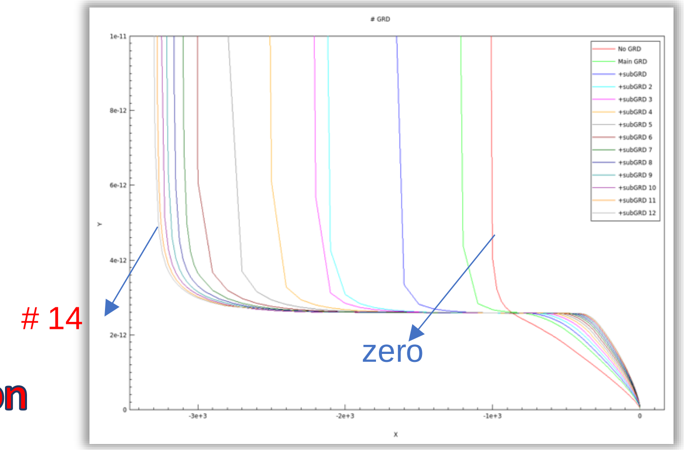
Input parameter				
Temperature	300K		Doping density	
Bias voltage	0 ~ -700V		(blue)	P^+ Boron
Carrier lifetime	e^-	$1\times10^{-4}s^{-1}$	(green)	N^- Phosphorus
	hole	$3\times10^{-4}s^{-1}$	(red)	N^+ Phosphorus

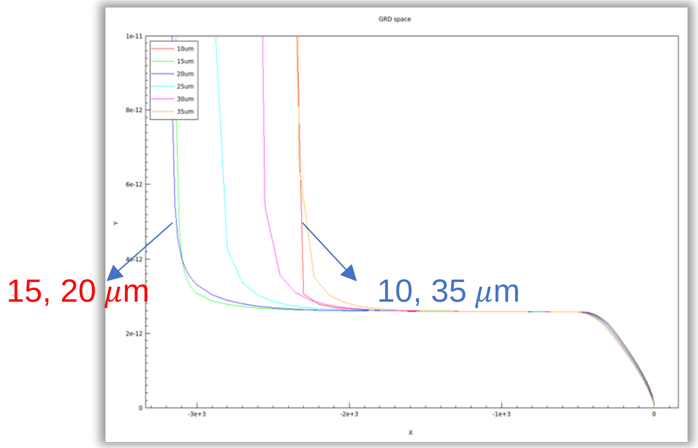
Leakage current simulation





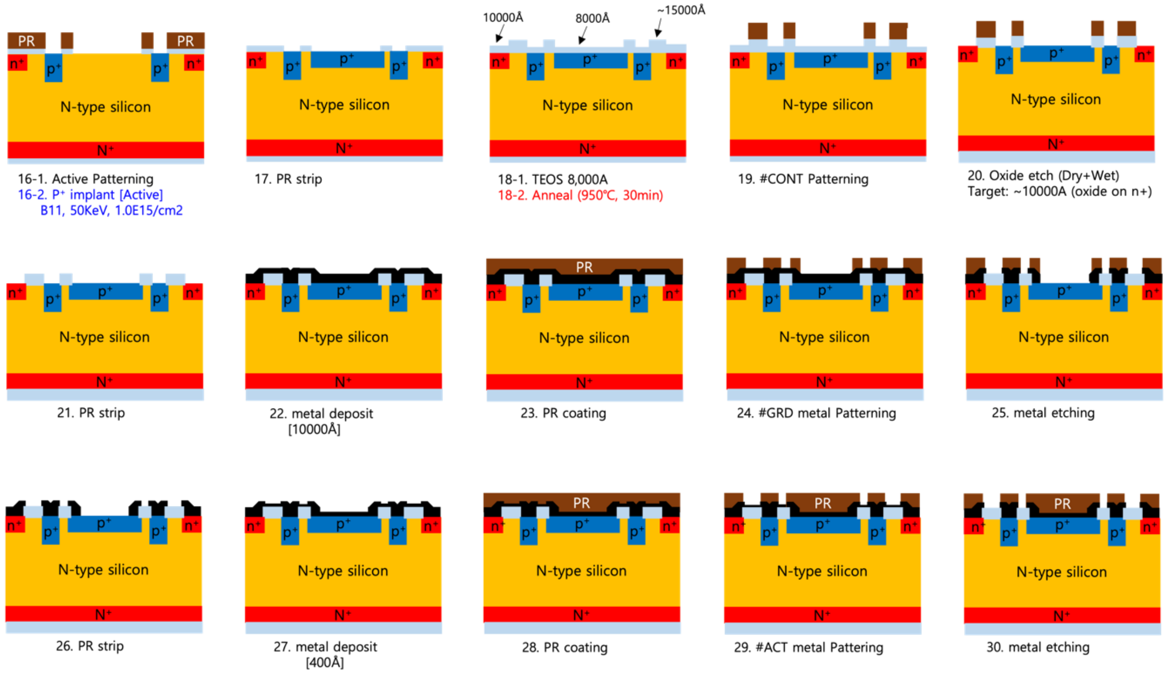
Breakdown simulation

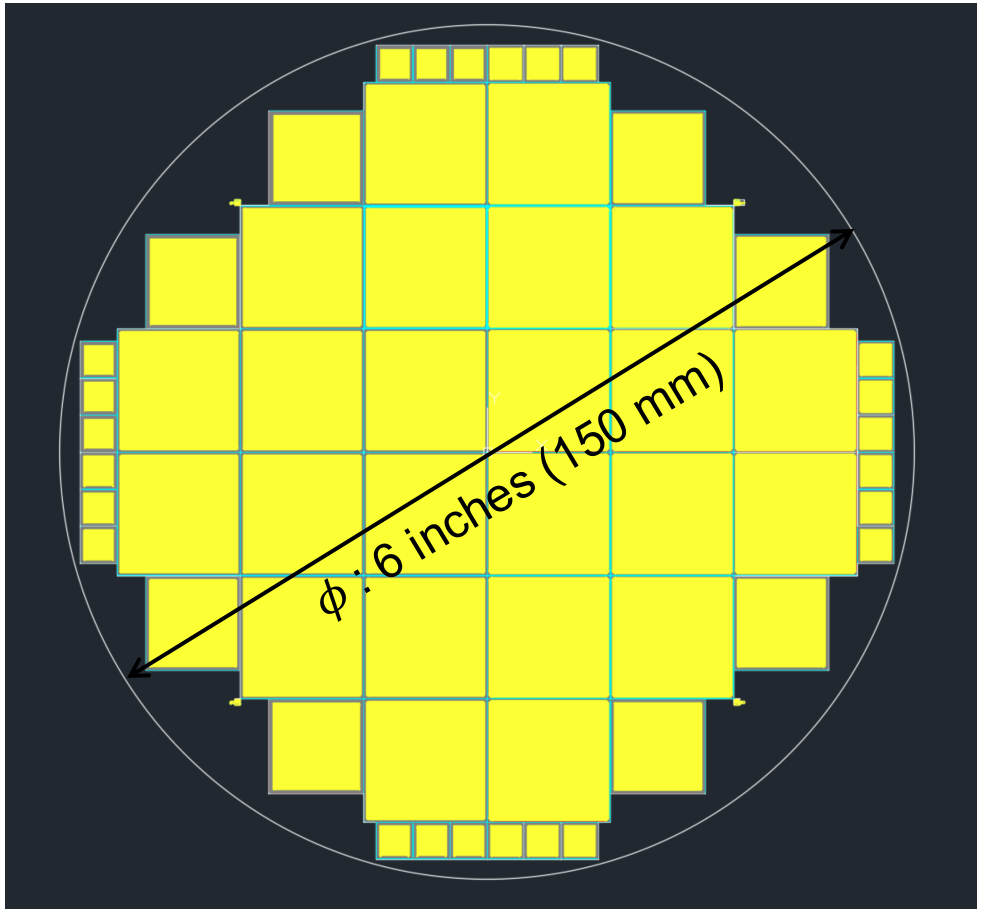




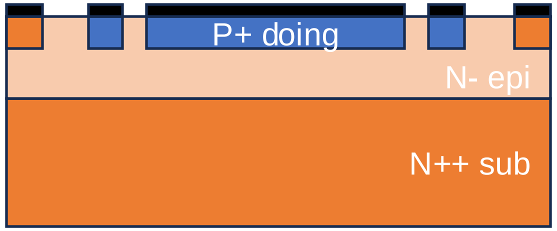
Si sensor production requirement

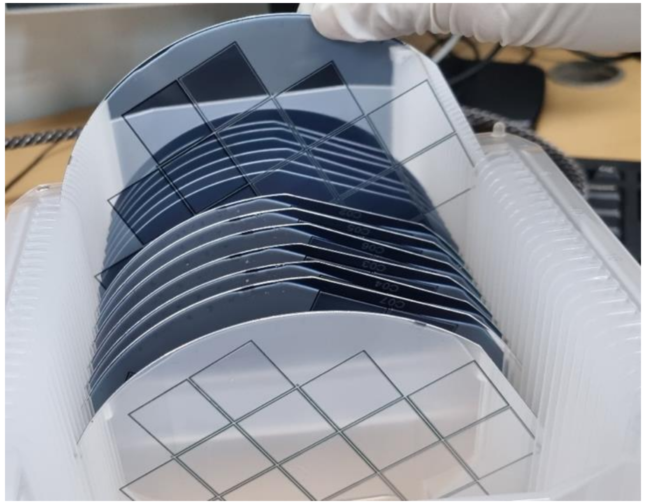
- Silicon process flows are designed in stages that involve information on the thickness of oxidation, metallization, or etching processes, as well as ion doping density
- To create patterns over an entire wafer at each step, photomasks are designed and fabricated

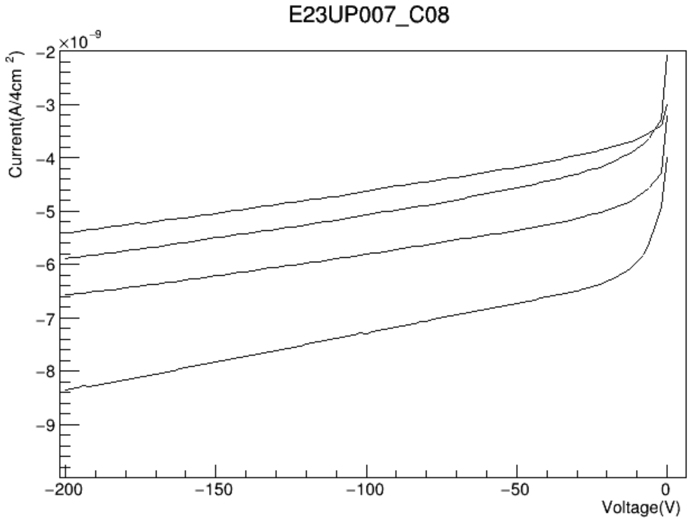


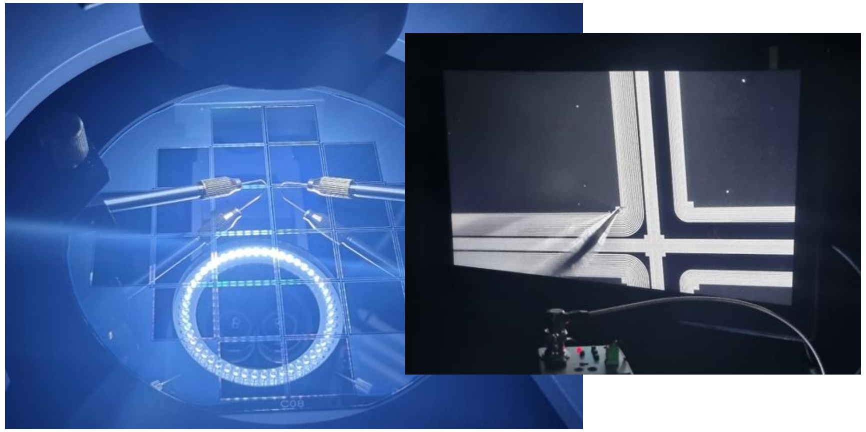


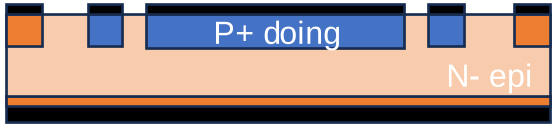
Thin(115 μm) sensor development

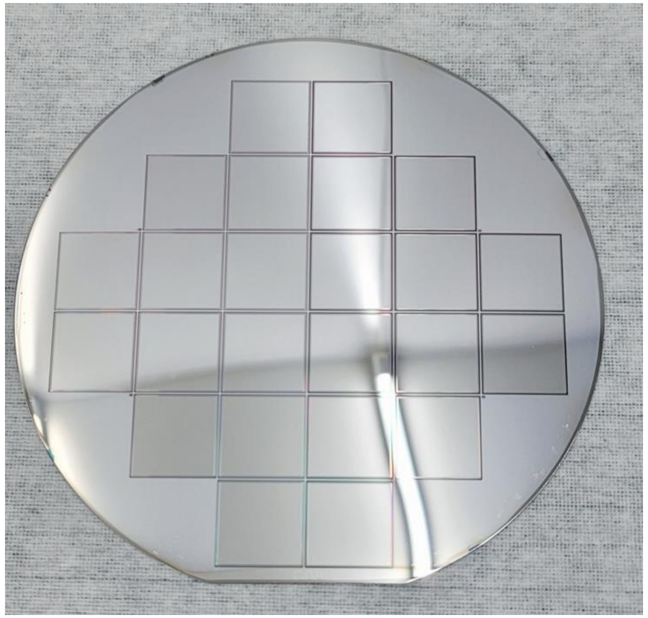












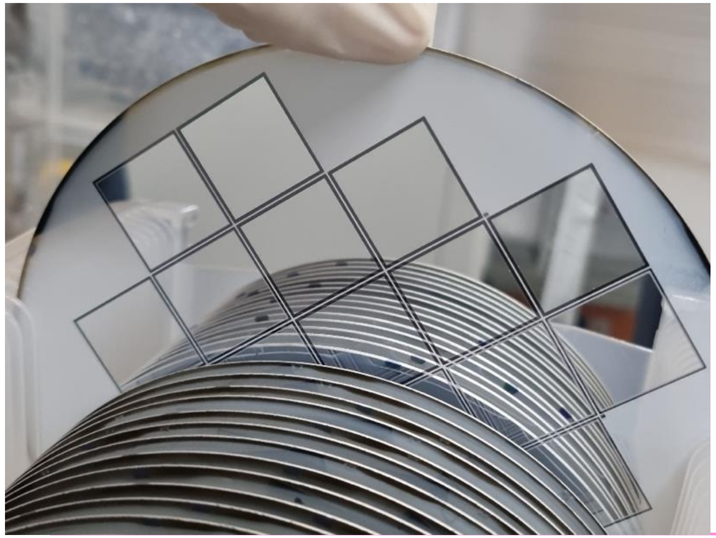
Pre-process
on epitaxy wafer

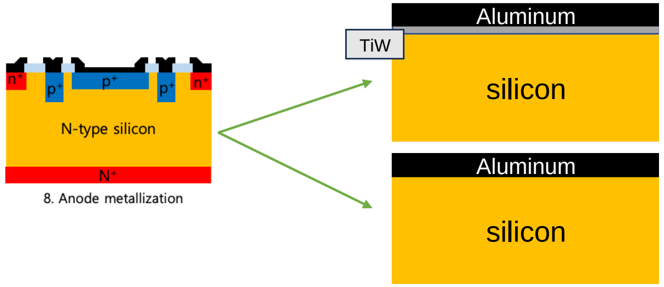
Wafer level test

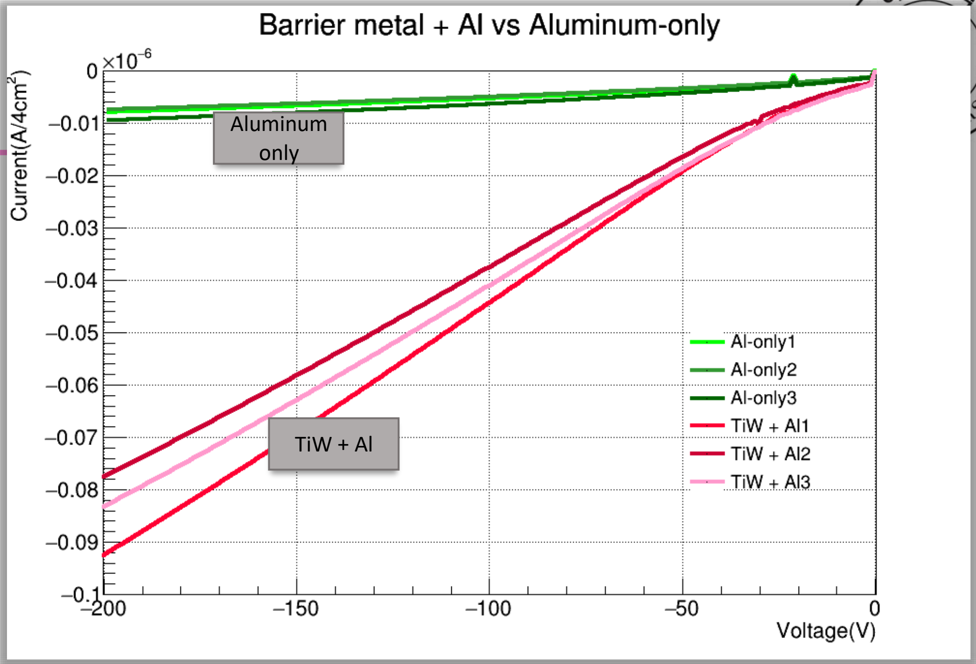
Post-process
(BG & BM)

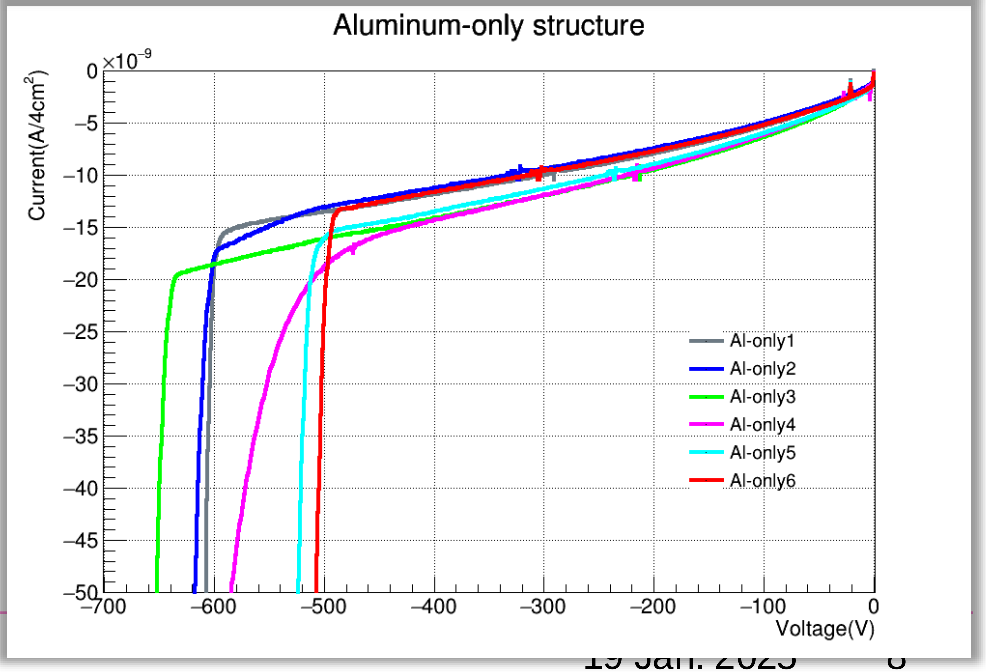
I-V measurements - barrier metal

- To assess the impact of the barrier metal on the anode, fabrication was conducted both with and without the barrier metal
- The tests were done using the thick sensor (750 μm thickness)
- The presence or absence of the barrier metal influenced the variation in leakage current
- Sensors exhibited breakdown voltages around –500 V



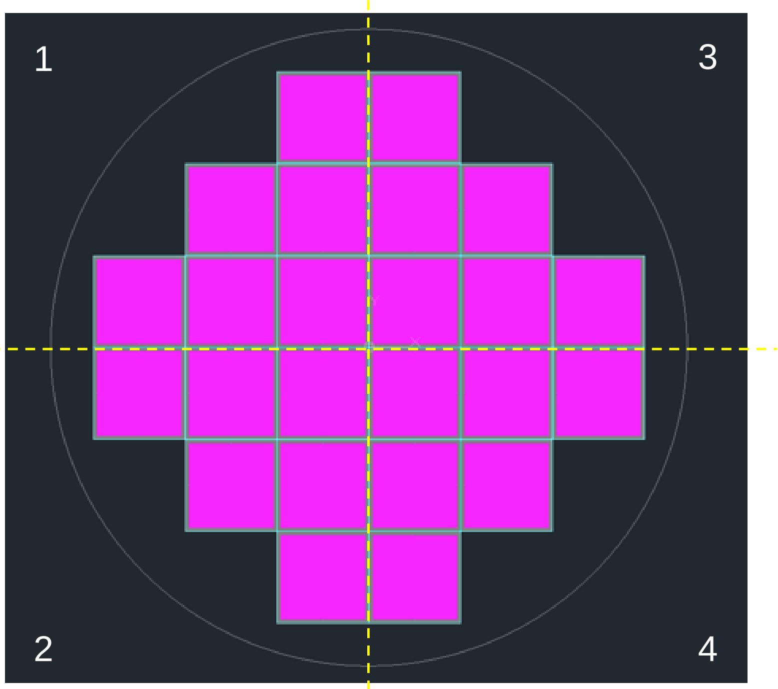


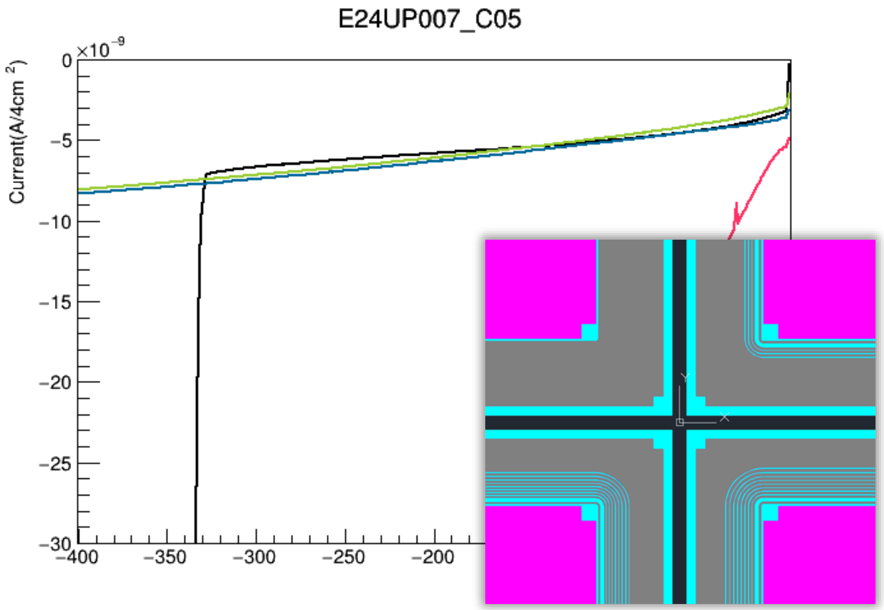


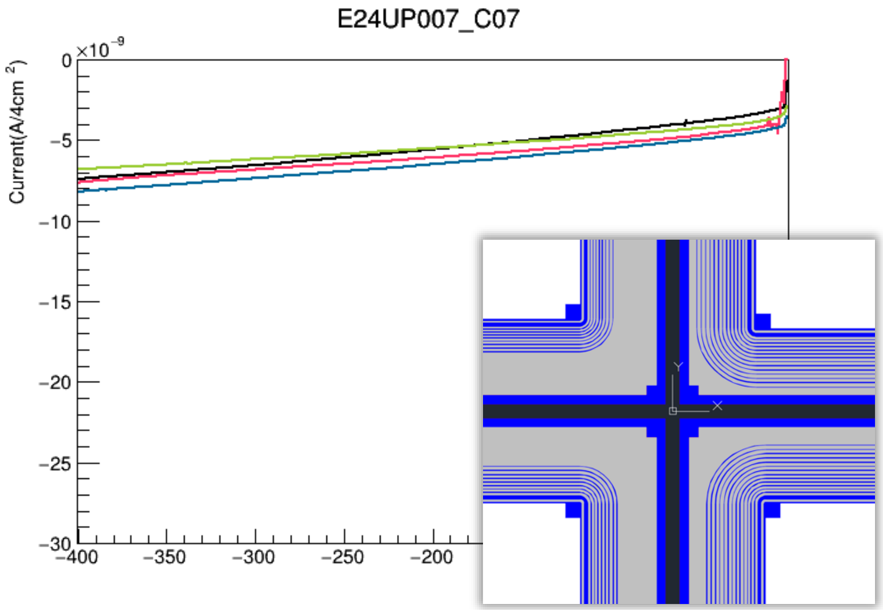


I-V measurements – exploiting different designs

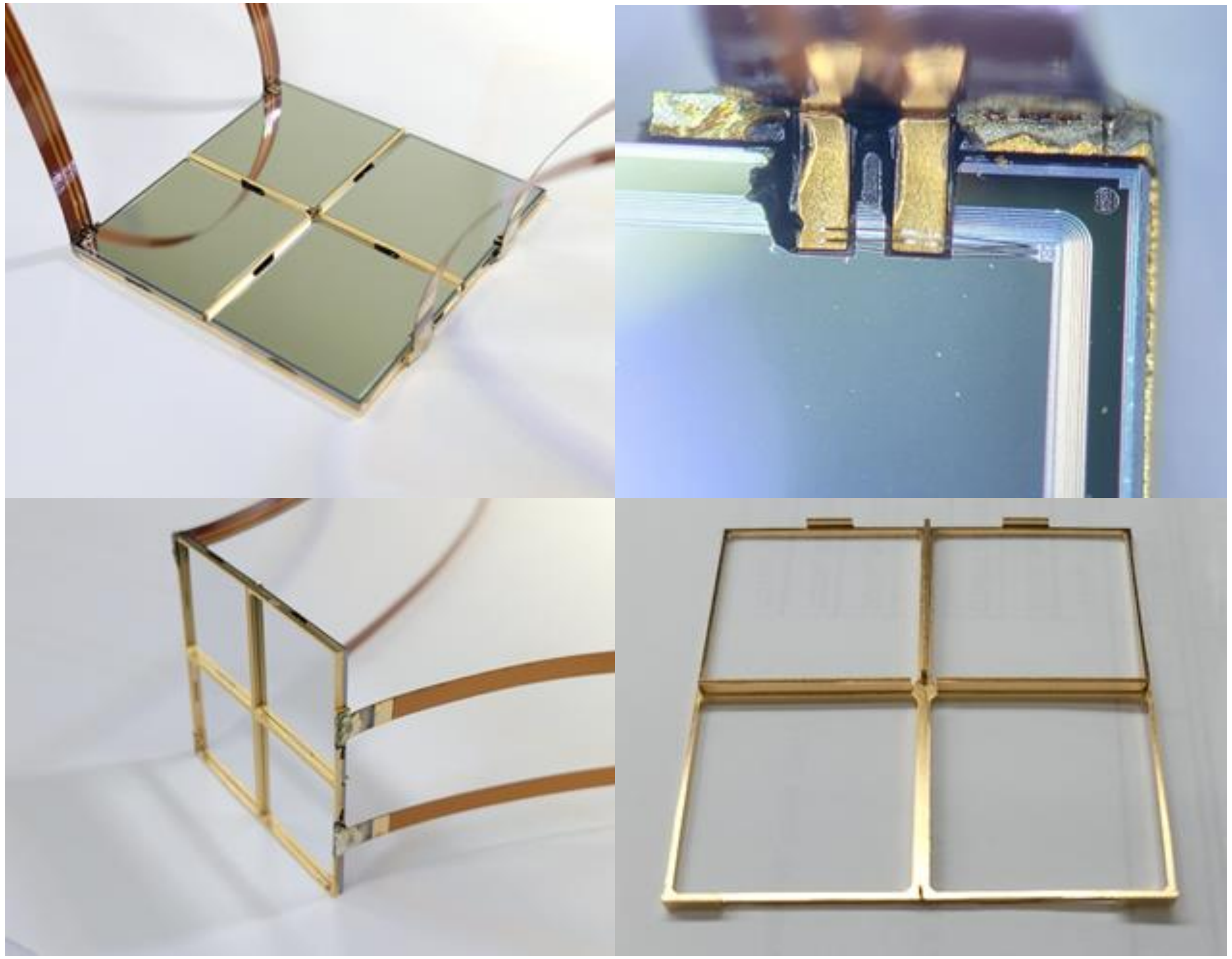
- To evaluate the impact of various guard ring patterns, eight different sensor designs were fabricated.
- The tests were done using the thin sensor (115 μm thickness), with the photomasks divided into 2x2 matrices
- The leakage current of each chip was measured to be less than 10 nA/cm^2



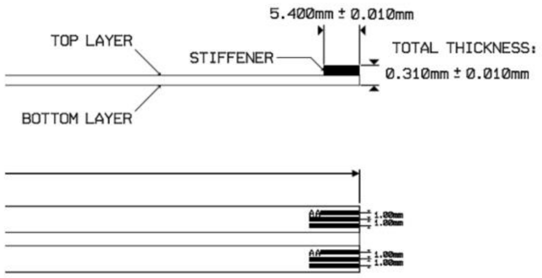




Chip assembly (by MEMSPACK)

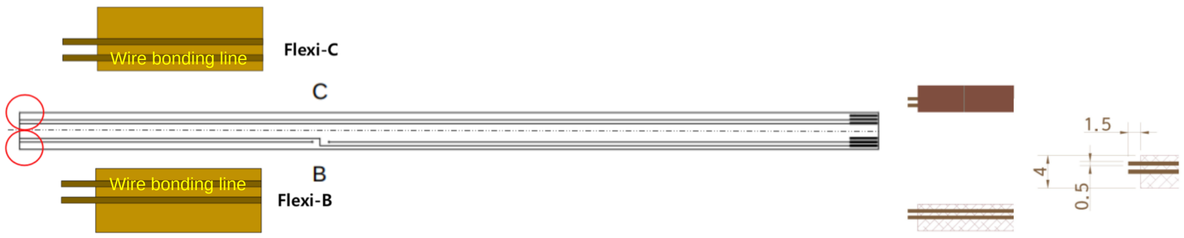


- Required components including the FPCB, Quartetto frame, and chips, were successfully manufactured in Korea
- Assembly, including wire bonding was carried out in collaboration with a local company in Korea (MEMSPACK)



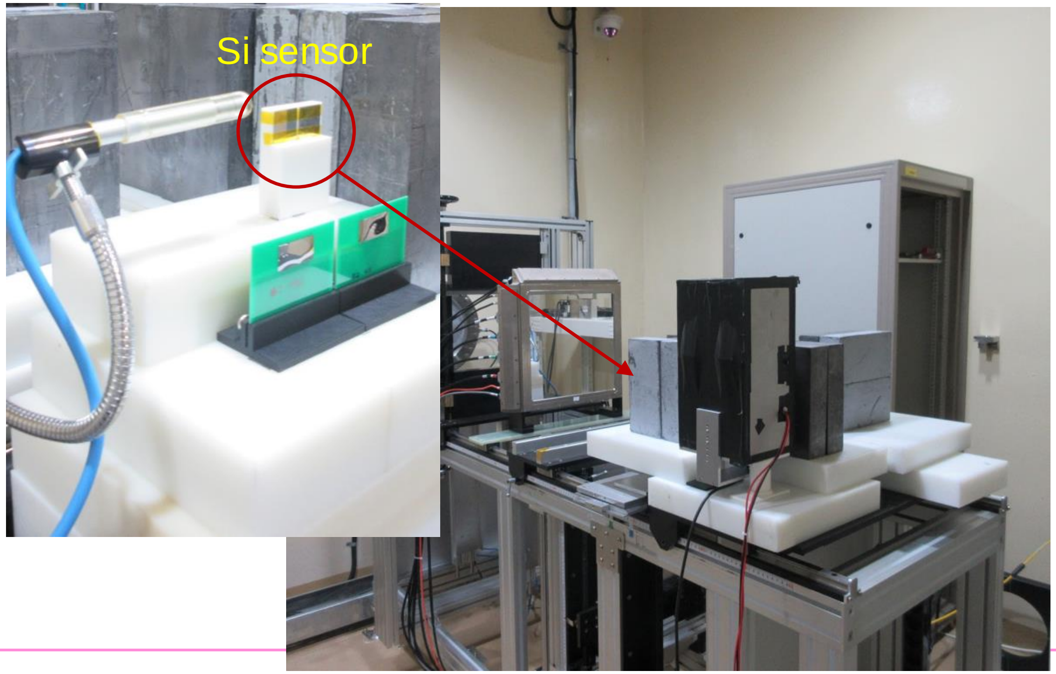
STACK UP	
THICKNESS	MATERIAL
150um	STIFFENER
25um	COVERLAY ADHESIVE
35um	COPPER
50um	POLYIMIDE CORE
35um	COPPER
25um	COVERLAY ADHESIVE
13um	COVERLAY

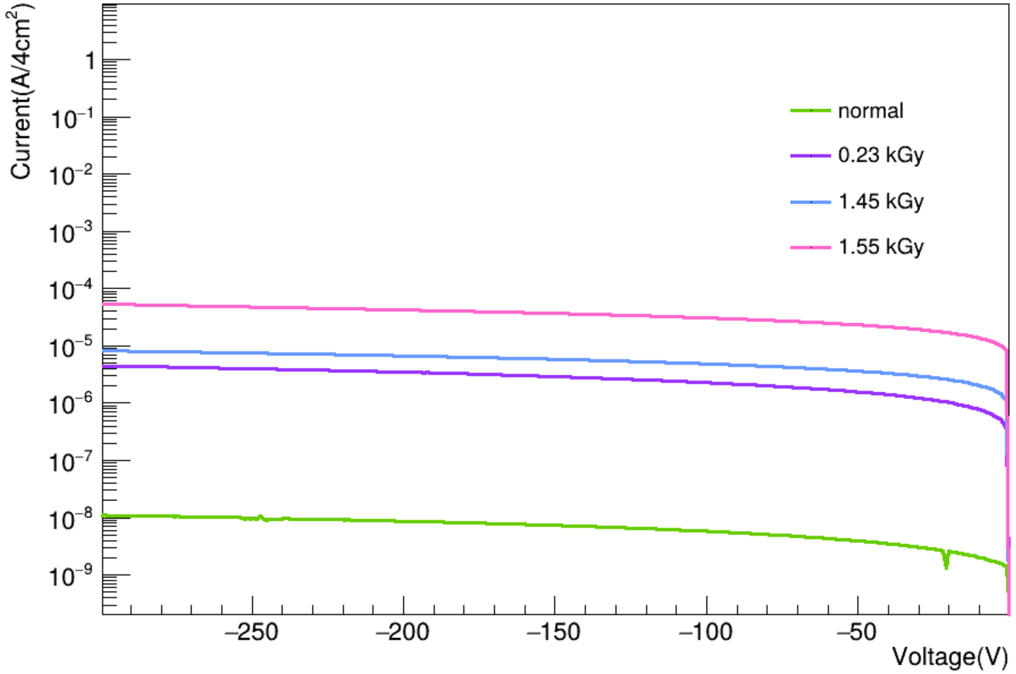
TOTAL THICKNESS 0.310mm ± 0.010mm



Radiation hardness test using proton beam (at KOMAC)

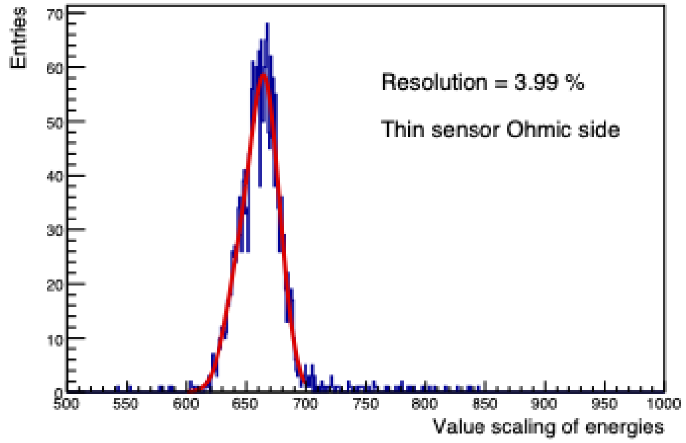
- KOMAC (Korea Multi-purpose Accelerator Complex) can provide proton beams at 25 ~ 100 MeV
- Satellite radiation hardness test were done using these sensors, with arbitrary radiation exposure level currently reaching up to 1.5 kGy
- Each 750 μm Si sensor was exposed to proton beams, resulting in an increase in leakage current corresponding to the extent of radiation damage

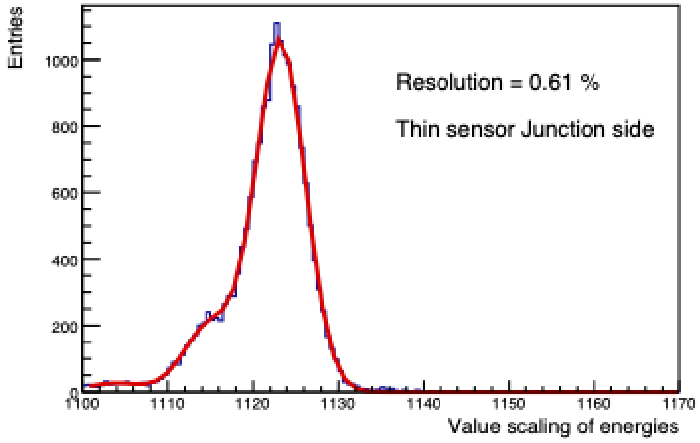


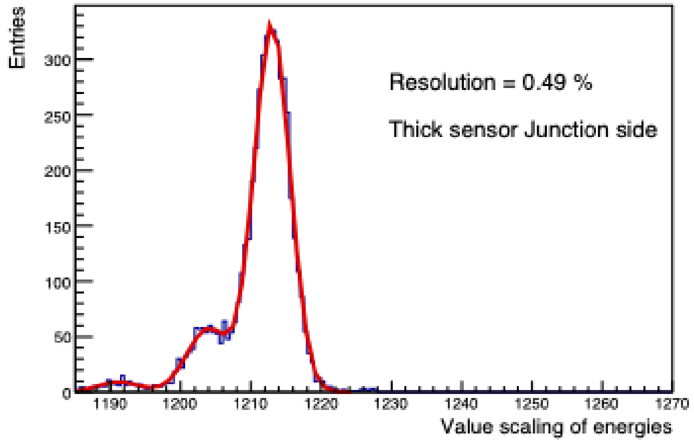


Energy resolution Test using Am-241 radiation source

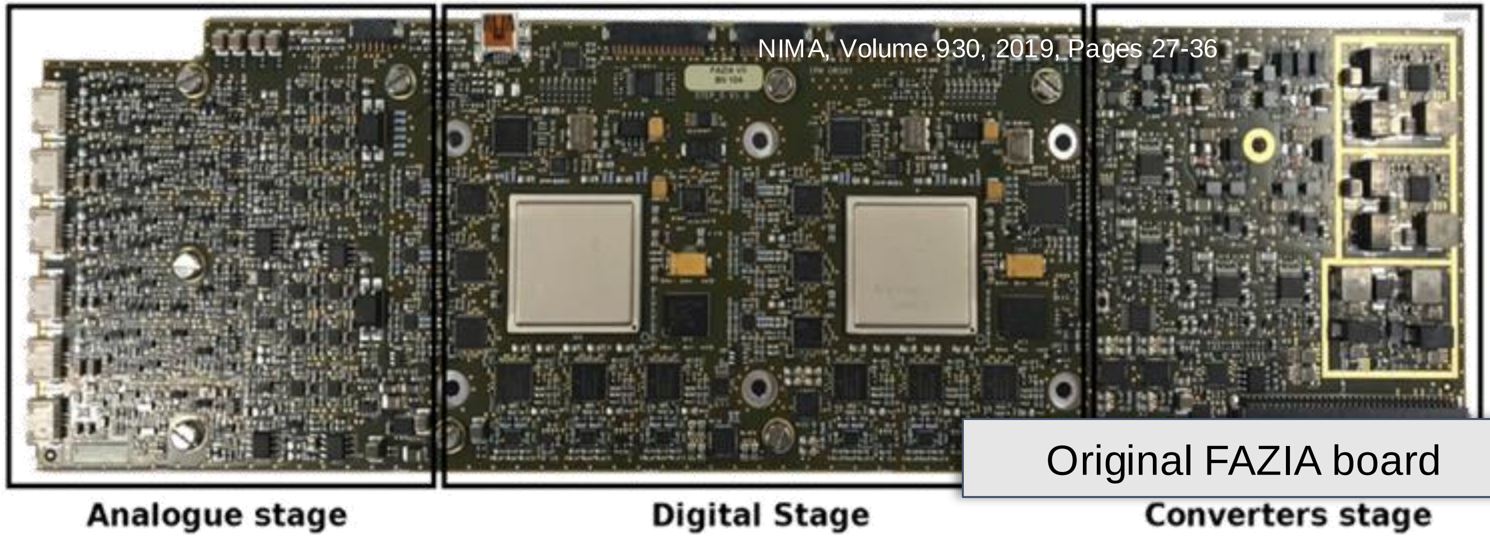
- The sensors were operated, and their energy resolution measured using charge-sensitive amplifiers and shaping amplifiers
- Output signals were read using a Flash ADC, where 1 count corresponds to 0.5 mV
- All measurements were conducted in a vacuum chamber
- The energy resolution of the sensors was measured to be approximately 0.5 %
- The resolution for Ohmic side injection of the thin sensors was measured to be approximately 4 %, and the resolution worsened due to the thick substrate on the Ohmic side.



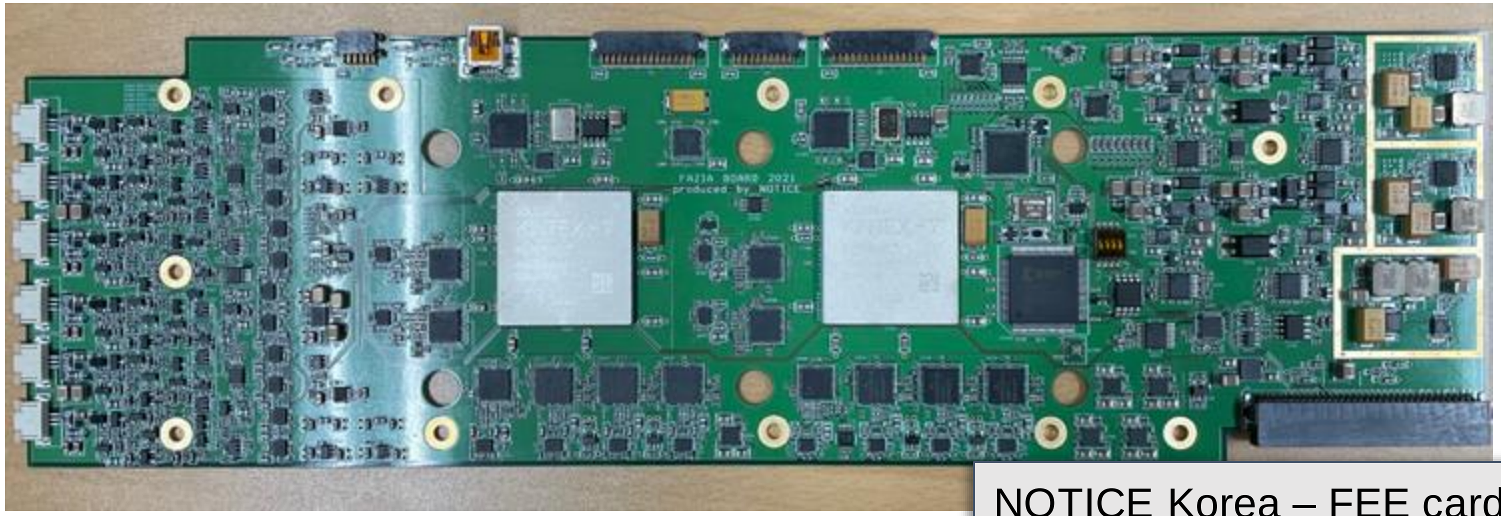




Front End Electronics board production (by NOTICE)



Original FAZIA board

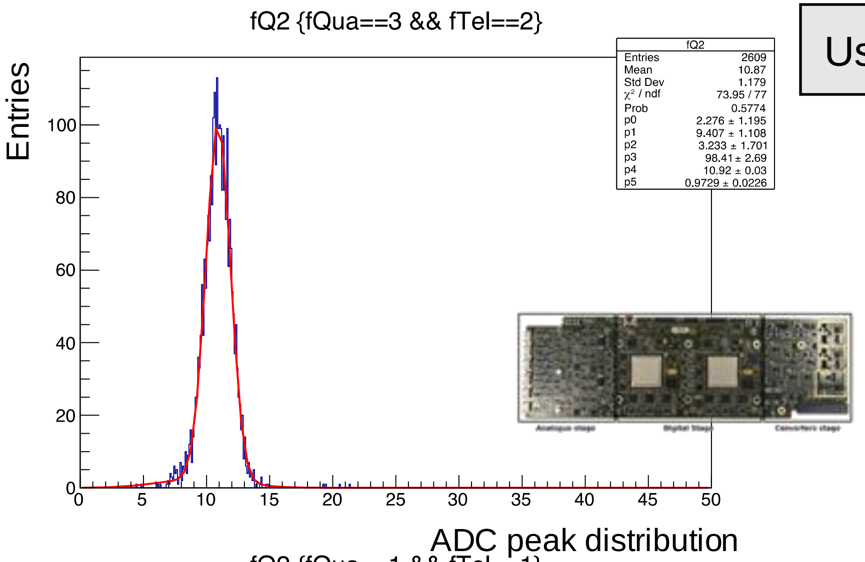


NOTICE Korea – FEE card

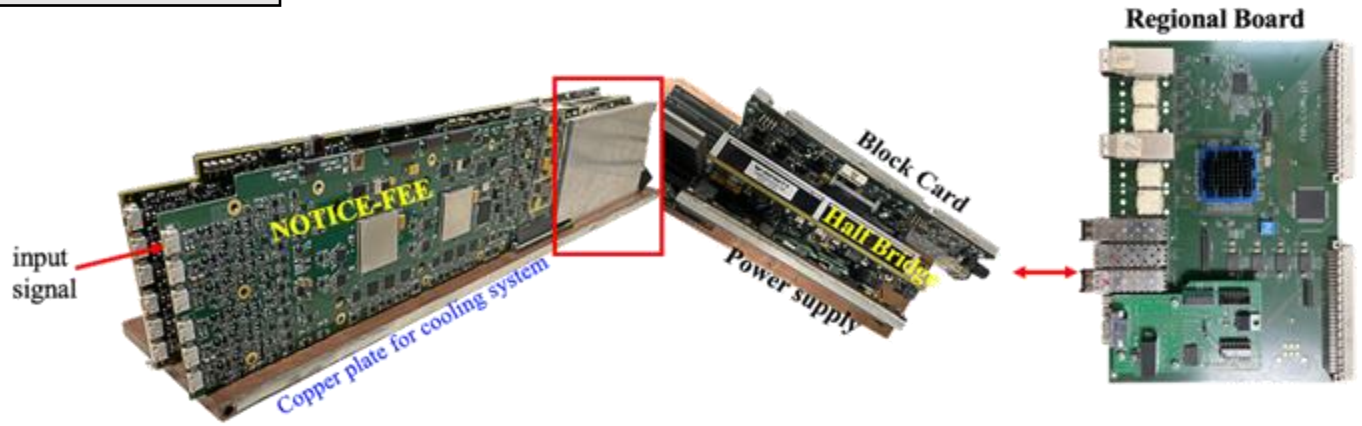
- **Analogue stage**:
  To amplify analog signals from the detector
- **Digital stage**:
  Signal processing of ADC (analog to digital converting) @ two FPGAs
- **Converter stage**:
  Power distribution and making bias voltage from LV

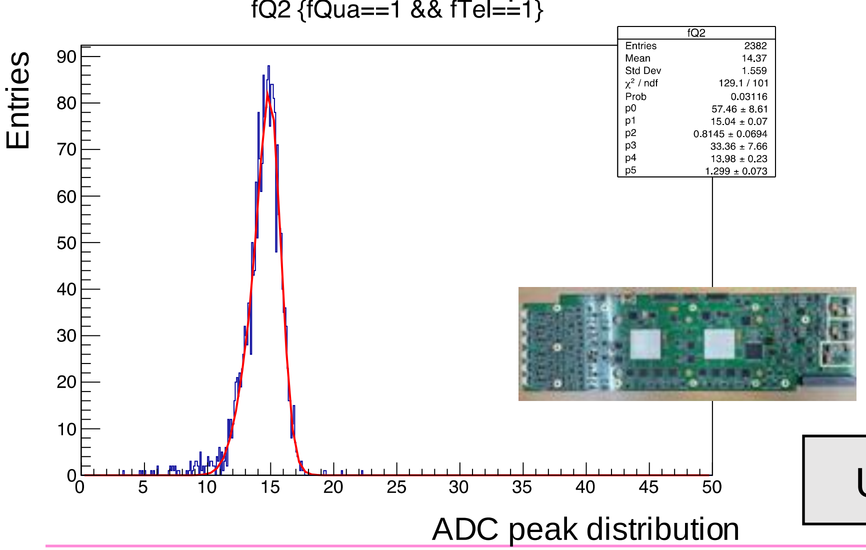
- Out-of-dated device were replaced
- New FPGA chips (Virtex-5 ➤ Kintex-7)
- New VHDL software developed
- Simple analogue stage was produced

New FEE board performance test using radiation source



Using current FEE board





- Am-241 radiation source test of FAZIA sensors with the FAZIA electronics (FEE, Block Card, and Regional Board)
- A total of 32 FEE cards were fabricated for four Blocks

Using new FEE board

Summary & outlook

- The R&D activity for the future FAZIA detector upgrade is ongoing, aiming to enhance its capability and expand the availability of FAZIA blocks in different places to benefit from any opportunities to perform excellent measurements
- R&D on sensor and FEE production are underway in Korea
- Radiation hardness tests were conducted using the KOMAC beam
- Radiation source tests were carried out using Am-241
- Basic Quality Assurance of FEE board ensured the successful production of the FEE boards
- Further investigations on silicon sensors will be performed for the upgrade in the FAZIA experiment
- The production of FEE boards and silicon sensors, configurable within one block, is ongoing

Acknowledgement

ETRI Electronics and Telecommunications Research Institute

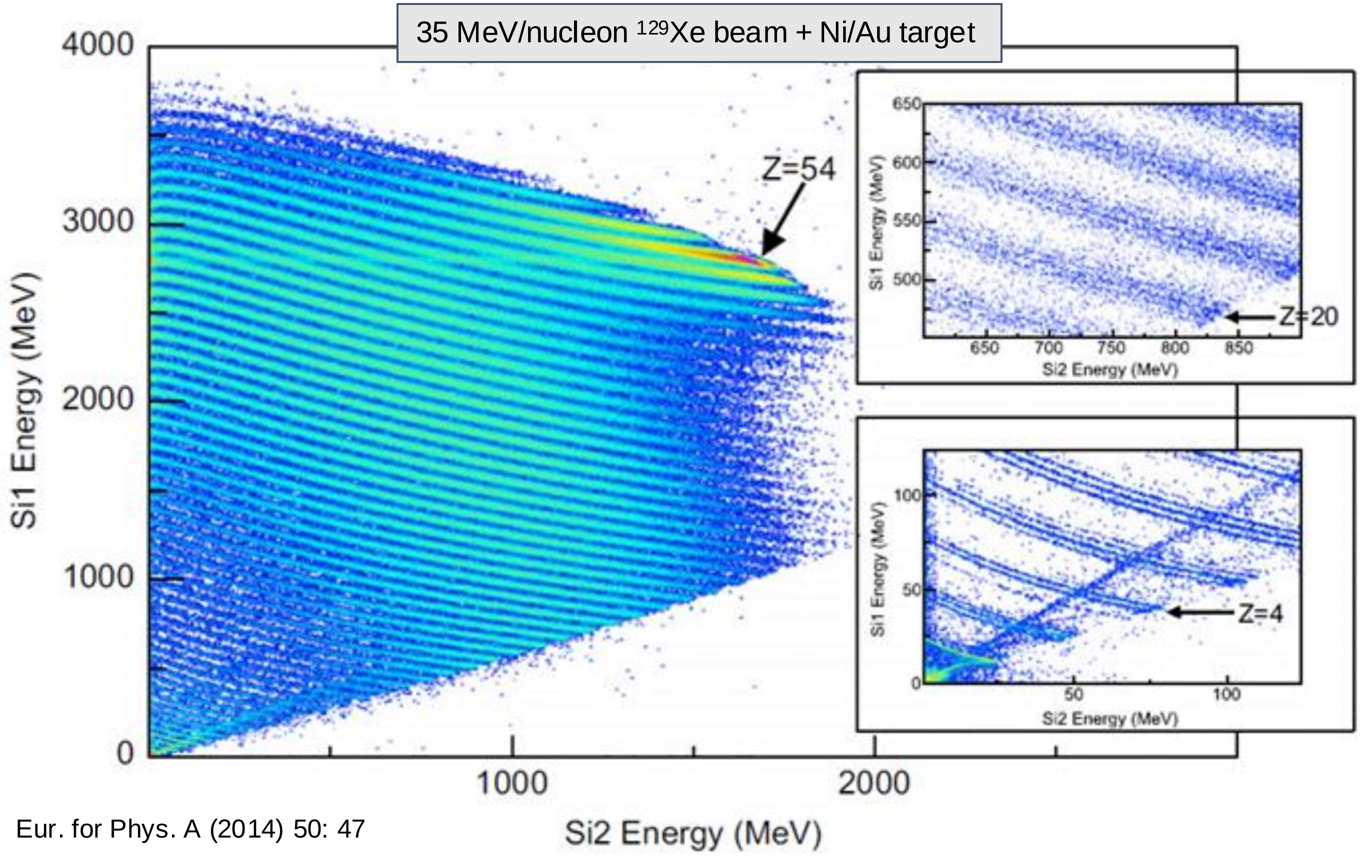
Nuclear and Optical Test Instrument and Communication Equipment NOTICE

MEMSPACK MEMS.IOT.Sensor

Thank you very much!

Back up

FAZIA PID performance



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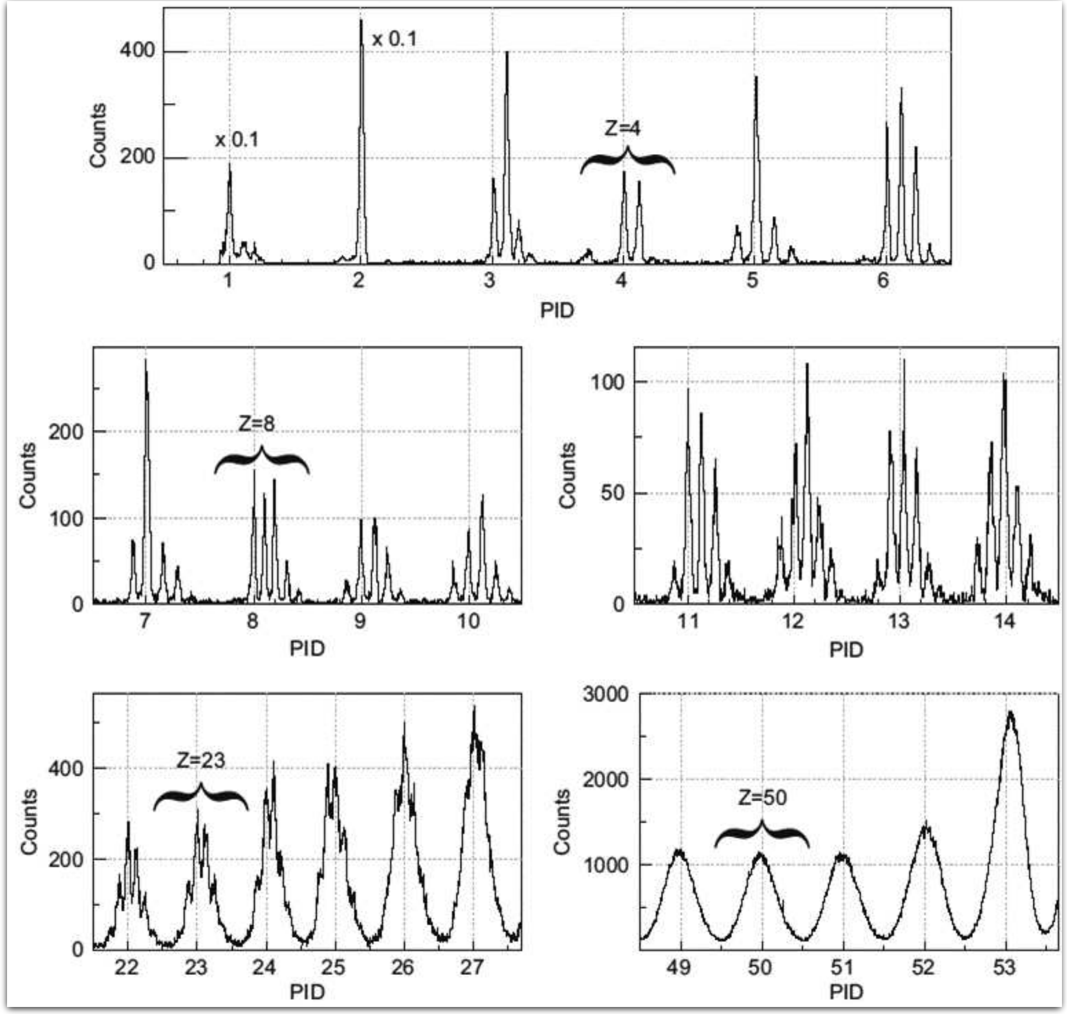
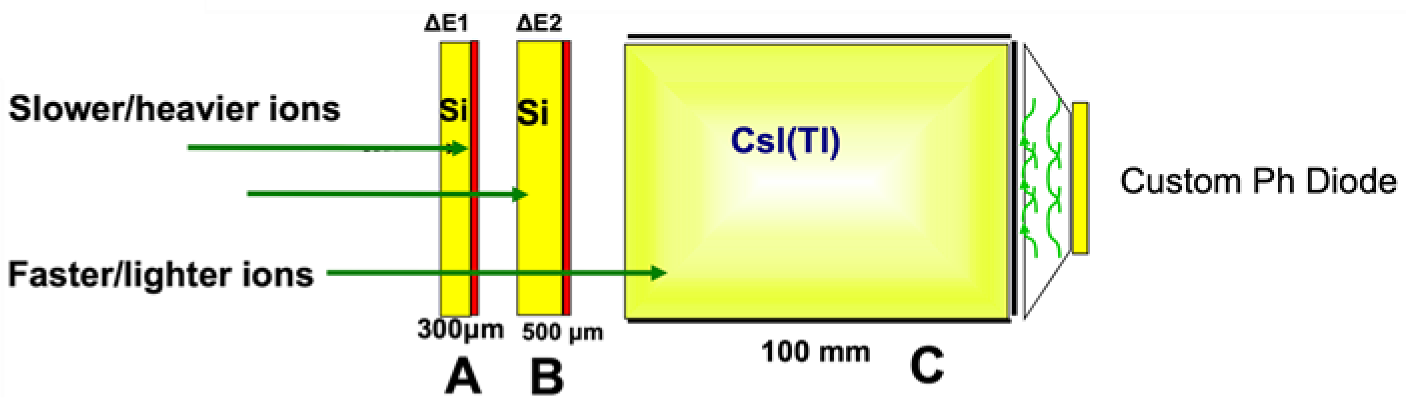
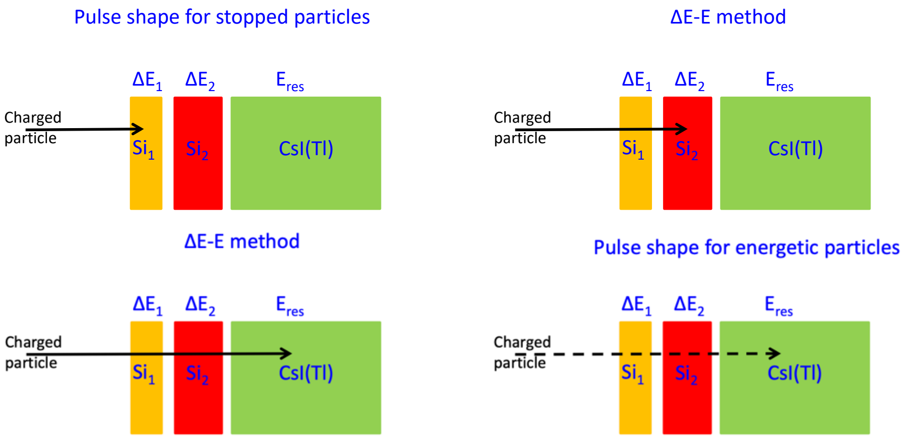


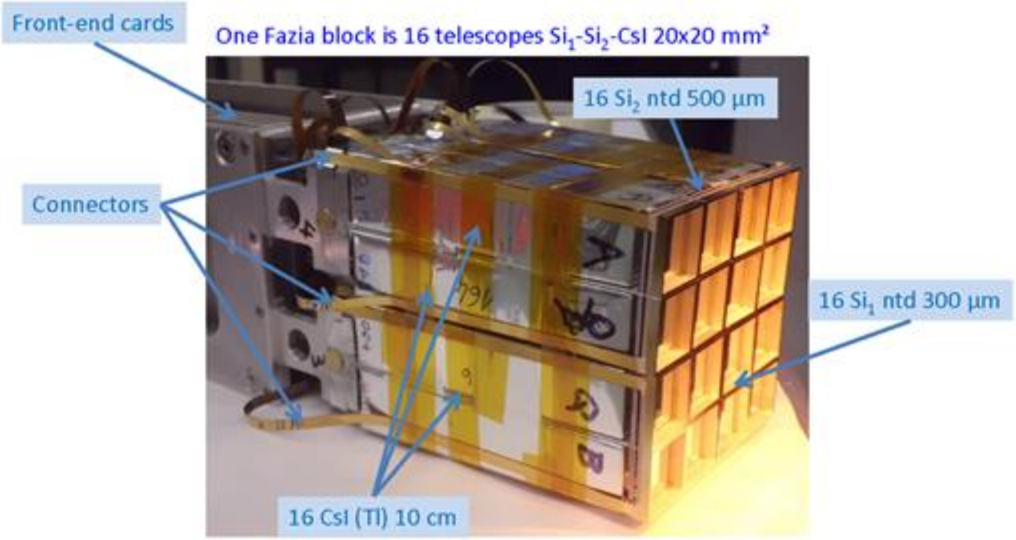
- ΔE - E charge identification has been tested up to Z ~ 54
- Clear mass discrimination up to Z ~ 26

The FAZIA telescope

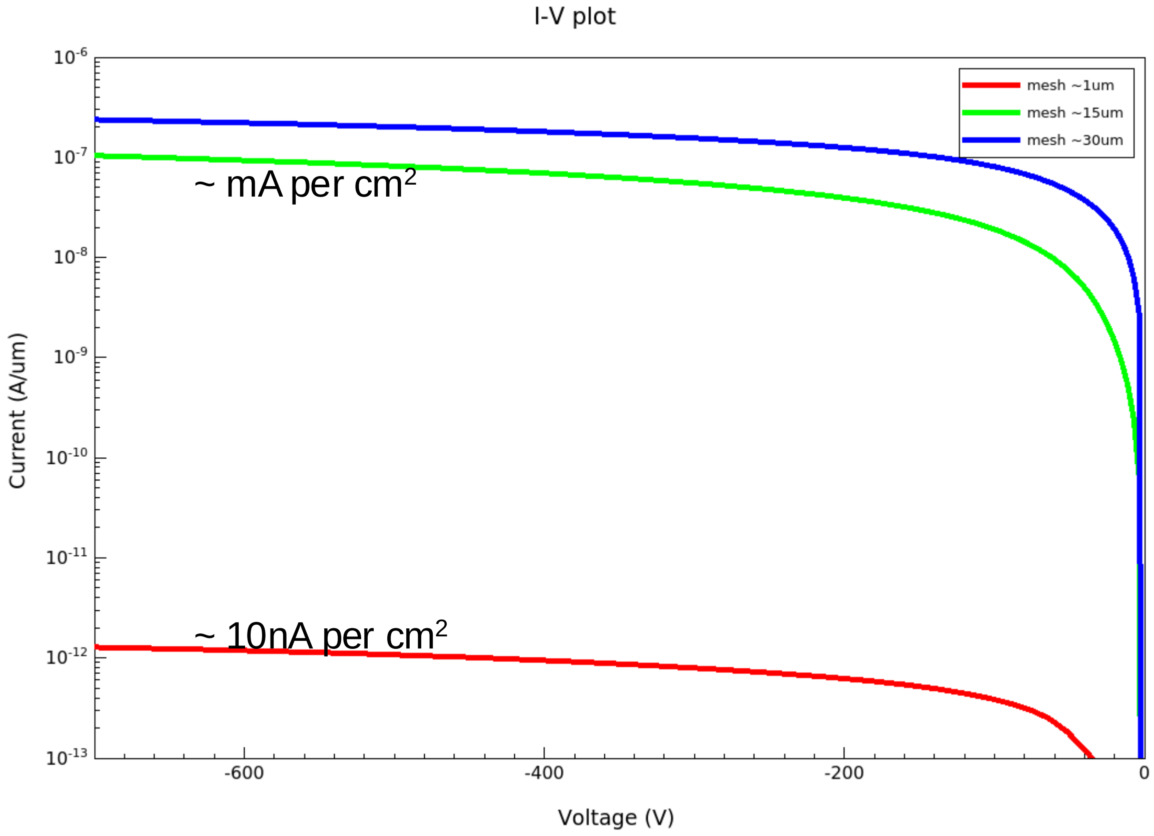




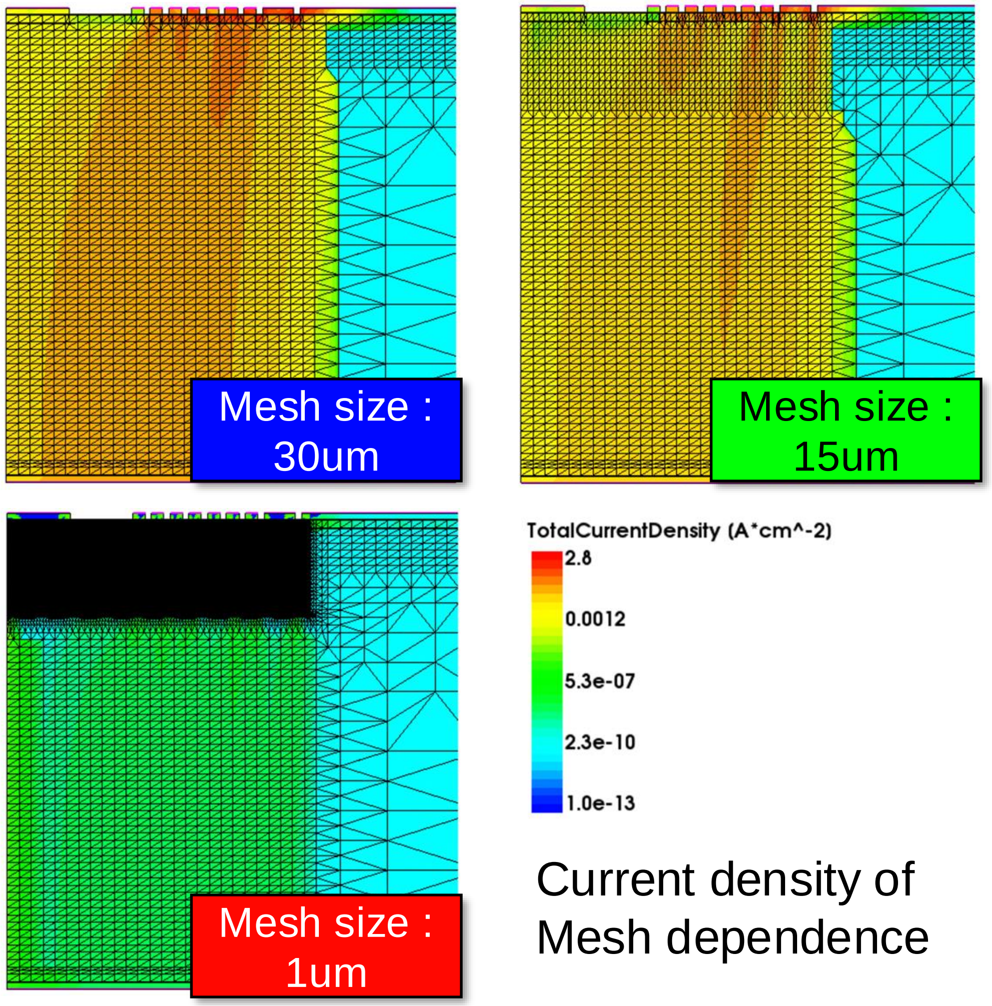
- One FAZIA telescope consists of Si1 + Si2 + CsI scintillator
  - Si1 : 2 x 2 cm^2, 300 μm thick
  - Si2 : 2 x 2 cm^2, 500 μm thick
  - CsI(Tl) : 2 x 2 cm^2, 10 cm thick
- One FAZIA block consists of 16 FAZIA telescopes
  - One Quartetto : 2 x 2 FAZIA telescopes
  - One FAZIA block : 2 x 2 Quartetto



Optimization of the calculation

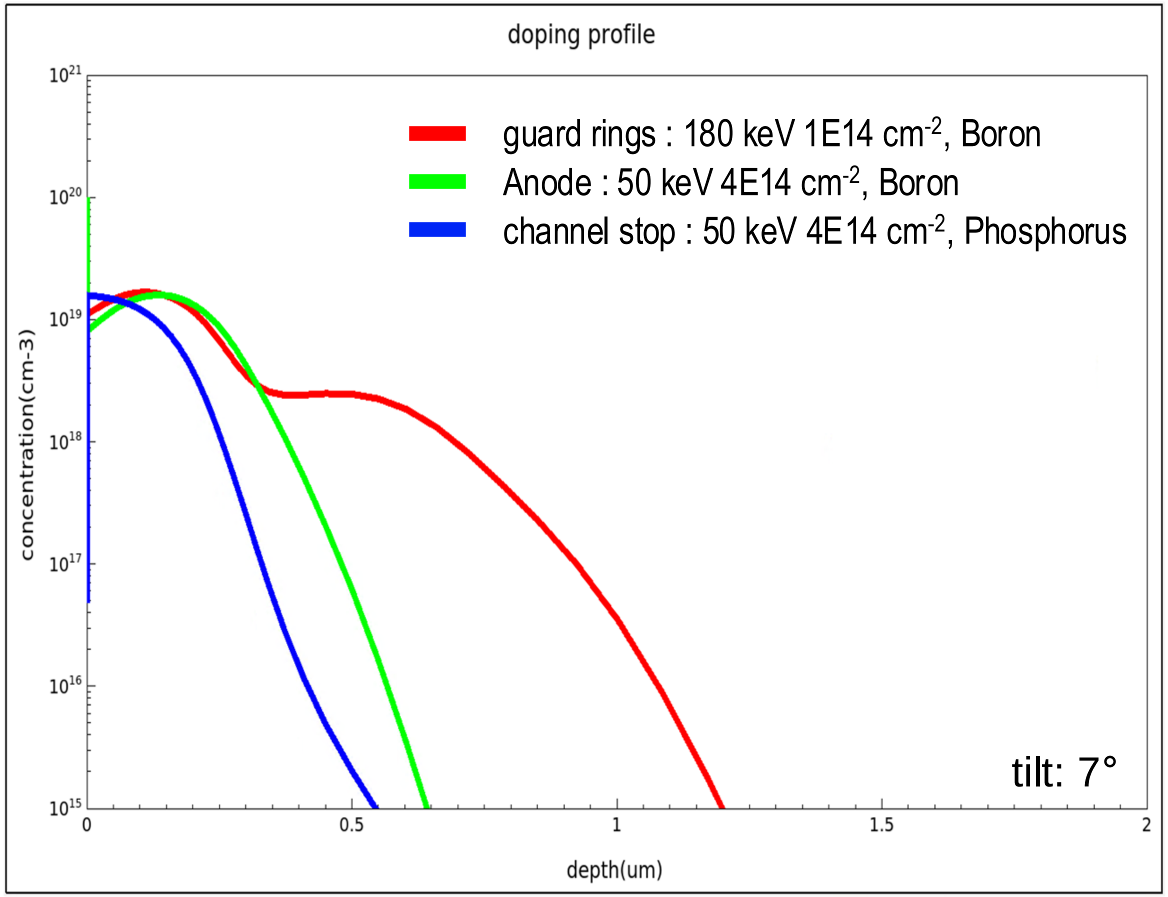


Calibration of 2-D silicon structure
electric current – reverse bias voltage plot



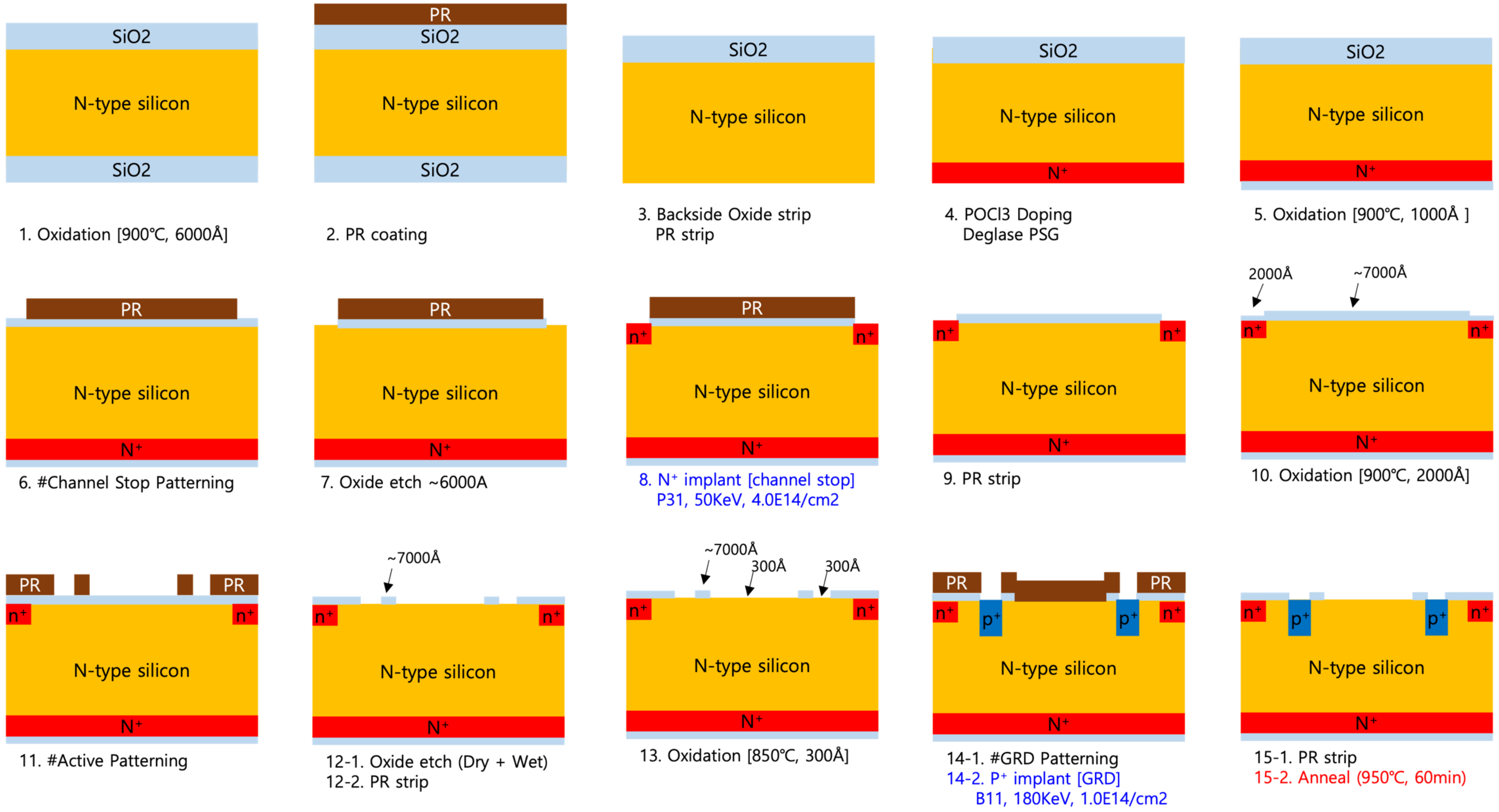
Current density of
Mesh dependence

Doping profile for ion implantation process

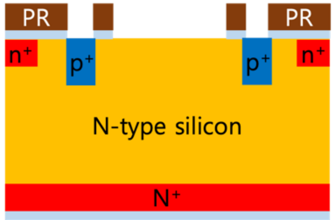


- Using TCAD tools, we simulated the ion implant process
  - The activation for the guard ring and channel stop region was performed at 950°C for 60 minutes
  - The activation for the anode region was performed at 950°C for 30 minutes
- To ensure completely Ohmic contact, we changed the dose value from 4E14 to 1E15 cm^{-2} in the anode region during the actual silicon process

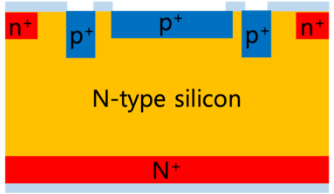
Process flow 1



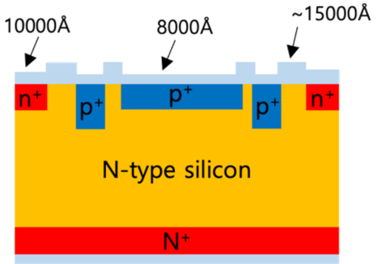
Process flow 2



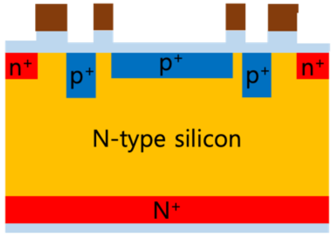
16-1. Active Patterning
16-2. P^+ implant [Active]
B11, 50KeV, 1.0E15/cm2



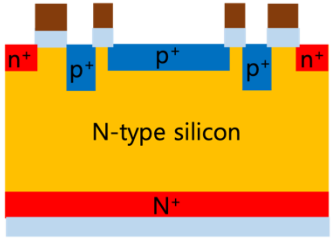
17. PR strip



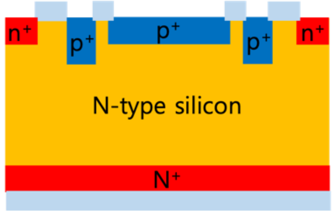
18-1. TEOS 8,000A
18-2. Anneal (950℃, 30min)



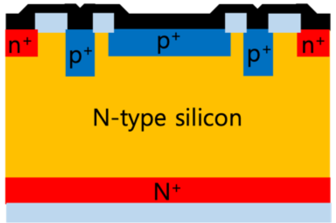
19. #CONT Patterning



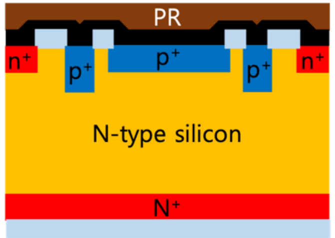
20. Oxide etch (Dry+Wet)
Target: ~10000A (oxide on n+)



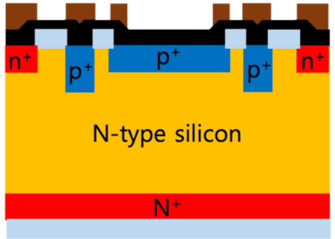
21. PR strip



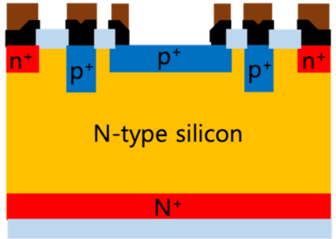
22. metal deposit
[10000Å]



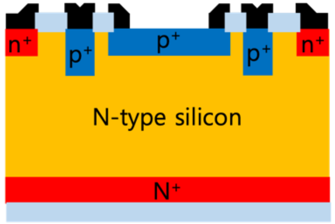
23. PR coating



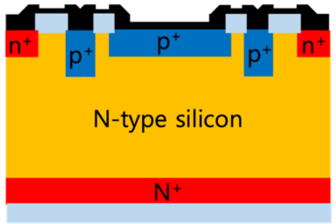
24. #GRD metal Patterning



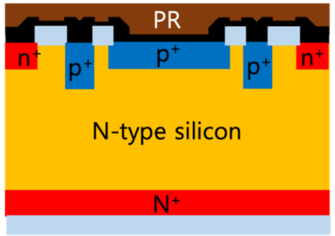
25. metal etching



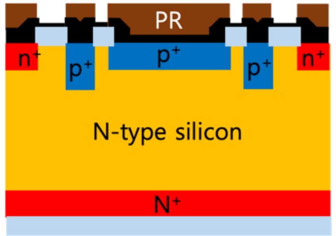
26. PR strip



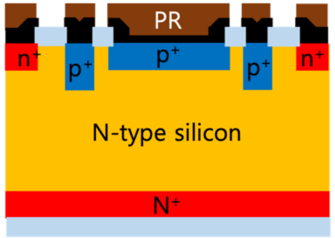
27. metal deposit
[400Å]



28. PR coating

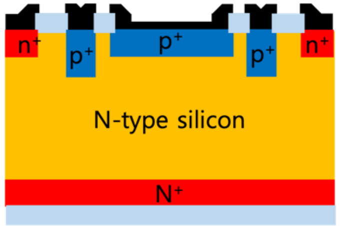


29. #ACT metal Pattering

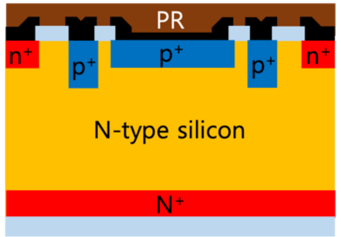


30. metal etching

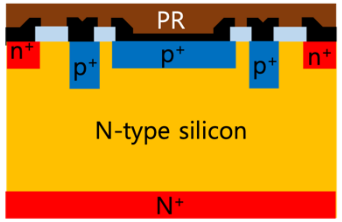
Process flow 3



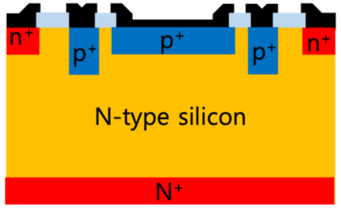
31. PR strip



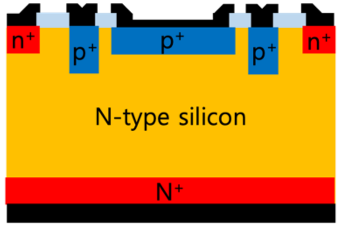
32. PR coating



33. oxide etching



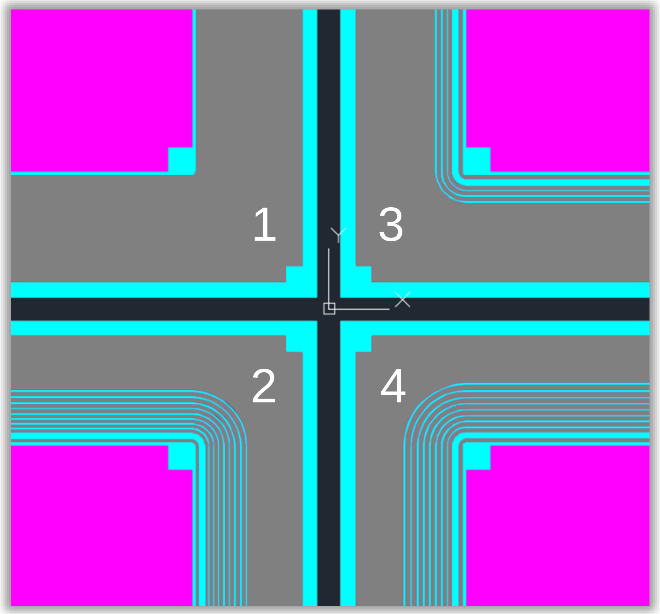
34. PR strip

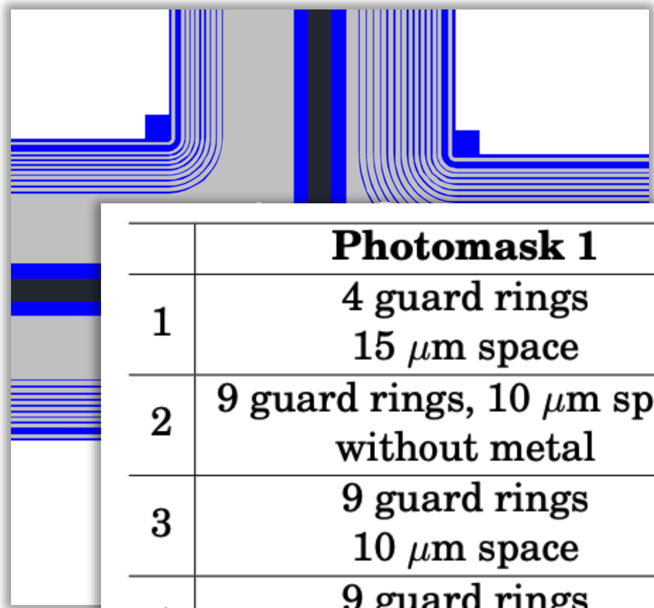


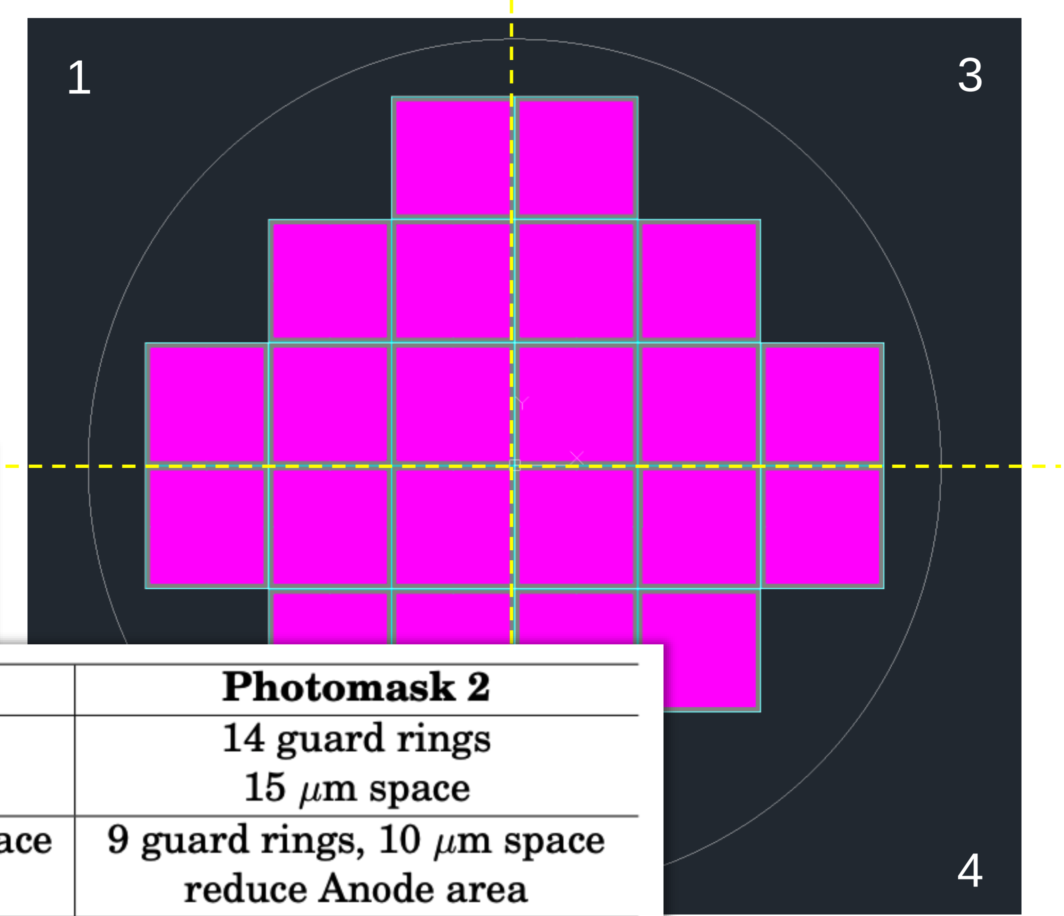
35-1. metal deposit [10000Å]
35-2. Alloy (420℃, 30min)

2nd: Different designs in one wafer

- Design the photomask with two different patterns
- Each photomasks has 4 different patterns on 4 sides
- In total, 8 different chip variations will be produced



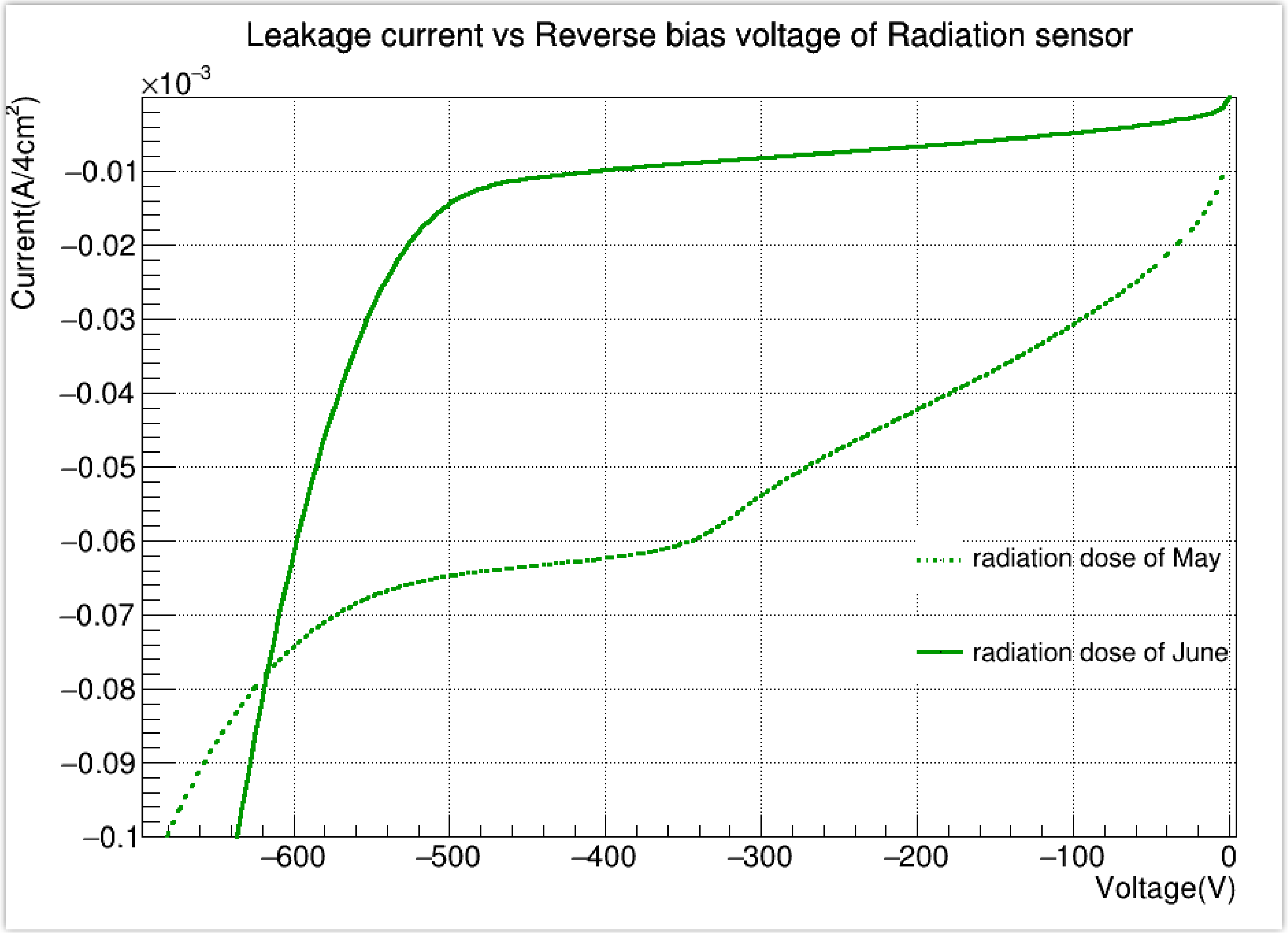




	Photomask 1	Photomask 2
1	4 guard rings 15 μm space	14 guard rings 15 μm space
2	9 guard rings, 10 μm space without metal	9 guard rings, 10 μm space reduce Anode area
3	9 guard rings 10 μm space	9 guard rings, 15 μm space reduce Anode area
4	9 guard rings 15 μm space	14 guard rings, 15 μm space reduce Anode area

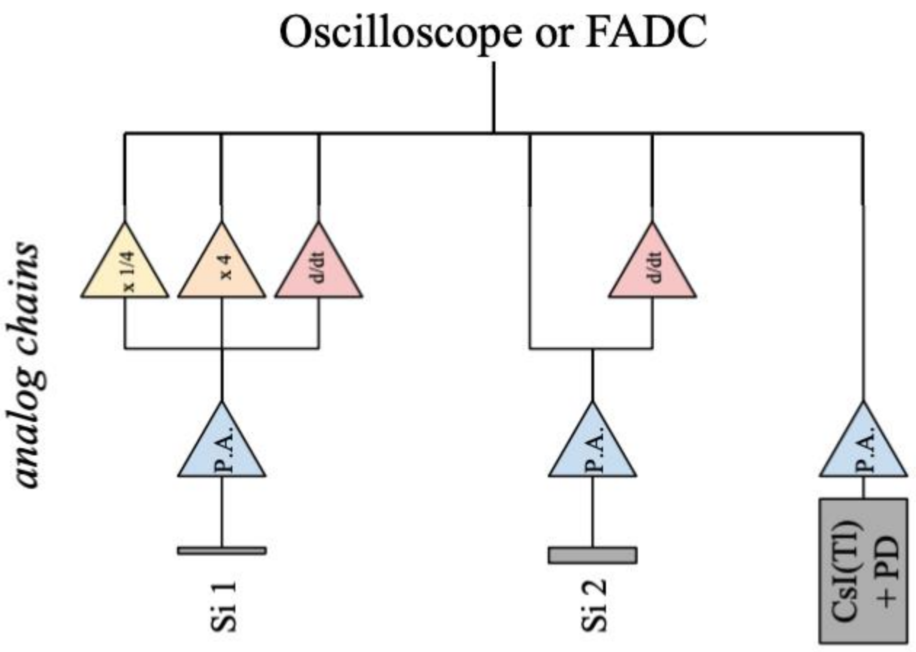
sk layout,
Ye0ngCha/Photomask_Layout

Breakdown property of irradiation sensors



Analog FEE card

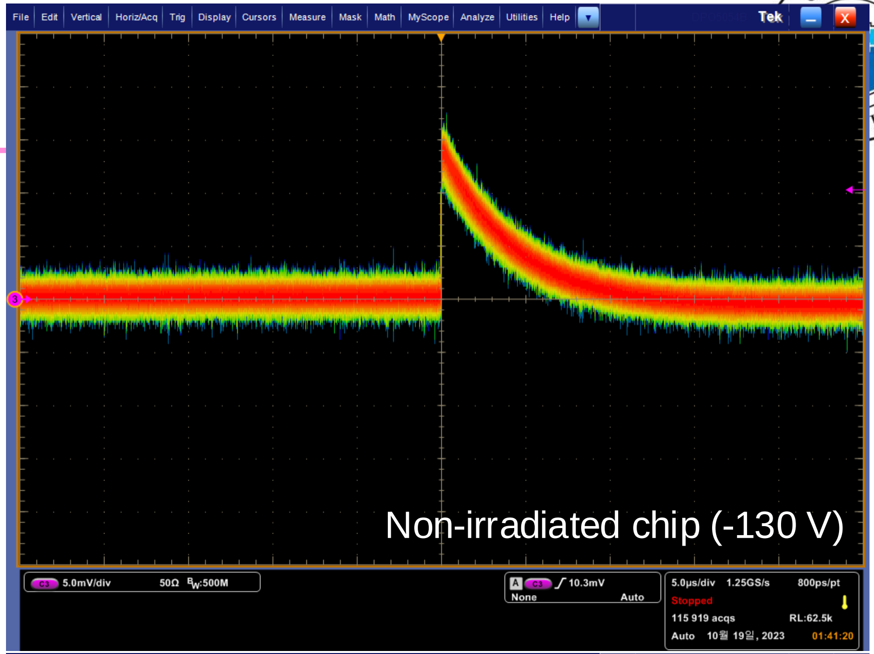
NOTICE-FEE analog board

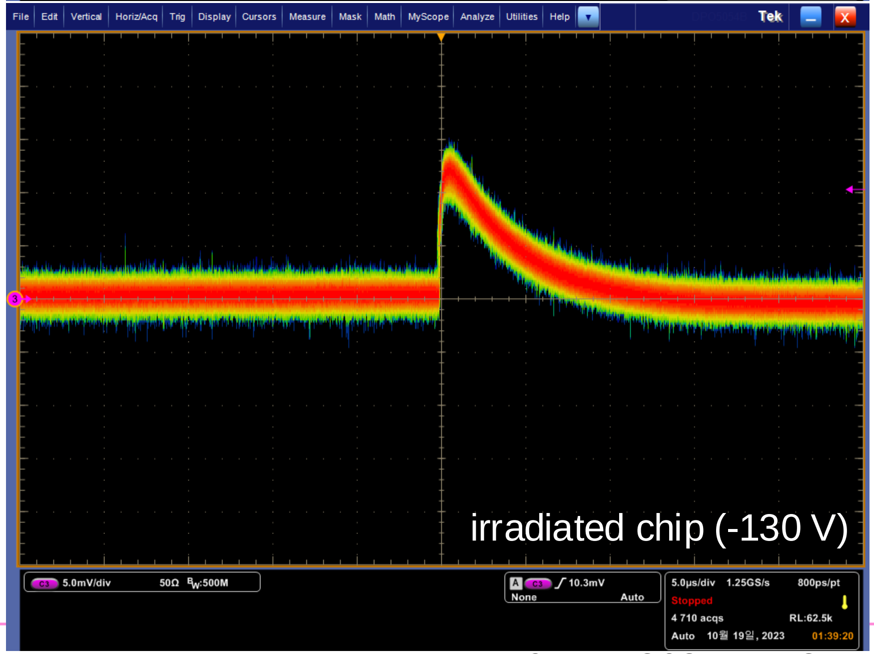


- Analog FEE card development for the Si chip test
  - Extraction of analog signals
  - Signals connection with Oscilloscope (or FADC) : SMA cable
  - Alpha source test

Source test using Am-241

- Reading and operating used Analog FEE cards, which amplify the signal by 4 times
- Confirming electrical signal to our silicon sensors using Am-241 radiation source
- Output signal of the irradiated chip decreased in peak value when it compared to the Non-irradiated chip (16 mV ➤ 14mV)





Energy resolution Test using Am-241 radiation source

- Energy resolution measurement were conducted using Am-241 source
- Output signals were measured using Flash ADC, where 1 count equates to 0.5 mV
- The measurement was carried out in a vacuum chamber
- FWHM of the 750 um chip was measured to be approximately 2 %