

# FAZIA Status Meeting

-Jeonghyeok Park-

## Board test - MCU(PIC) main 함수

### Initialize

```
while (!both_fpga_ok)
{
    get_data_fpga1 = (UINT) (getid() << 1); -> 0
    wrspi(1, 0x02, get_data_fpga1); -> 0
    wrspi(2, 0x02, get_data_fpga1 + 0x01); -> 1

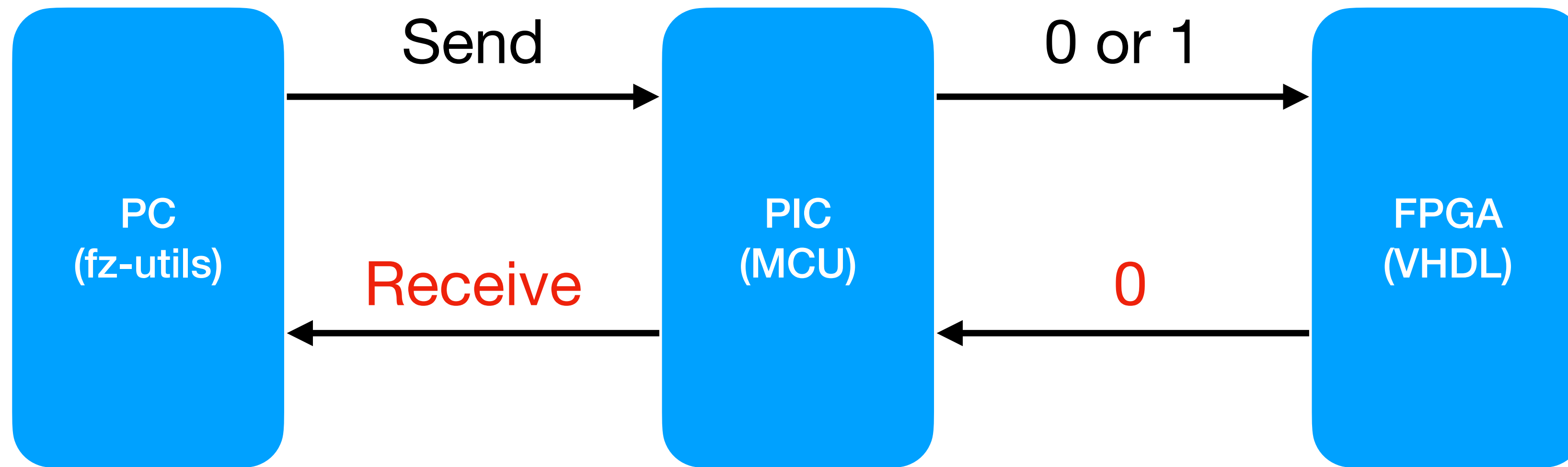
    rd_data_fpga1 = rdspi(1, 0x02);
    rd_data_fpga2 = rdspi(2, 0x02);

    if ((rd_data_fpga1 == get_data_fpga1) && (rd_data_fpga2 == get_data_fpga1 + 0x01)) {
        both_fpga_ok = TRUE;
    }
} // end while
```

### Function

1. FPGA (A,B)에 0,1 신호를 보낸다.
2. FPGA (A,B)에서 신호를 읽는다.
3. 두 FPGA에서 보낸 신호와 읽은 신호가 같으면 다음 작업을 실행한다.

# Board test flow













# Board test - GitHub

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 JeongHyeokPark Changed tel\_a to telA 7167fe9 4 hours ago 6 commits

 FPGA_uploader	Changed Name Of MCU To FPGA_uploader	6 hours ago
 common	The first commit for Kintex-7 VHDL code	6 hours ago
 simu	The first commit for Kintex-7 VHDL code	6 hours ago
 telA	Changed tel_a to telA	4 hours ago
 telB	Changed tel_a project to original name	4 hours ago
 tel_a	Changed tel_a project to original name	4 hours ago
 tel_b	The first commit for Kintex-7 VHDL code	6 hours ago
 .DS_Store	The first commit for Kintex-7 VHDL code	6 hours ago
 README.md	Add README	6 hours ago

<https://github.com/JeongHyeokPark/Kintex-7>

# BACKUPS